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Traditio et Innovatio

High-Power Hybrid Si/SiC Active Neutral Point Clamped Converter

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Ich versichere hiermit, die vorliegende Dissertation eigenständig und ausschließlich unter Verwendung der angegebenen Hilfsmittel angefertigt zu haben. Alle öffentlichen Quellen sind als solche kenntlich gemacht.

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Rostock, 27 March 2024 M.Sc. To Pham Ha Trieu

I would like to say a special thank you to Professor Eckel for his support and giving me a chance to work on this interesting topic. My passion for power electronics has come from his interesting lectures during my master study at university of Rostock. I appreciate for the precious time he spent with me just to show me how to write the first abstract submission. That is the starting point for all my publications.

I would like to thank all the colleagues, who helped me during my working here, in the power electronics lab.

Finally, I would like to express great appreciation to my wife and my family for always supporting me unconditionally during my Phd journey and in my personal life.

Abstract

Inverter with low output current ripple is necessary for many applications. Conventional IGBT based two-level inverter usually needs a bulky LCL filter at the output to suppress the high frequency harmonics. The filter volume can be significantly reduced if the three-level inverter is used and even better if it is switched at high frequency. The hybrid Si/SiC active neutral point clamped (ANPC) inverter is an ideal option for this solution. Thanks to the flexibility of different switching schemes, ANPC is able to relocate the fast switching devices to SiC MOSFETs and the slow switching devices to Si IGBTs. By doing so, the switching losses is strongly reduced at high switching frequency. The solution is not new for low power applications where all the switches are discrete devices connected on a small PCB or all the switches are integrated inside a module, which have low commutation loops' inductances. In high power applications, the concept has the main challenge of high commutation loops' inductances which limit the switching speed of the devices. There are two types of hybrid ANPC distinguished by the number of SiC MOSFETs are used: 4SiC and 2SiC hybrid ANPC. The 4SiC version is preferred for high power applications due to its small commutation loops of the high-speed SiC MOSFETs. In contract, 2SiC hybrid ANPC is impossible to use for high power applications because of its MOSFETs' long commutation loops. Actually, the long commutation loops can be decoupled by laying a decoupling capacitor near to SiC MOSFET. But the presence of the decoupling capacitor in the high power 2SiC hybrid ANPC topology poses many challenges in the design process and practical implementation. This dissertation is aimed to address those issues which are very specified for this topology. Additionally, designing a high-speed switching MOSFET presents its own set of challenges. Some novel and interesting solutions to those problems are also proposed in this dissertation. An experimental 500kW 2SiC hybrid ANPC was built and run continuously to prove those proof of concepts.

Zusammenfassung

Wechselrichter mit geringer Ausgangsstromwelligkeit sind für viele Anwendungen erforderlich. Herkömmliche IGBT-basierte Zwei-Pegel-Wechselrichter benötigen in der Regel einen sperrigen LCL-Filter am Ausgang, um die hochfrequenten Oberwellen zu unterdrücken. Das Volumen des Filters kann erheblich reduziert werden, wenn ein dreistufiger Wechselrichter verwendet wird, und noch besser, wenn er mit hoher Frequenz geschaltet wird. Der hybride Si/SiC-Active Neutral Point Clamped (ANPC)-Wechselrichter ist eine ideale Option für diese Lösung. Dank der Flexibilität verschiedener Schaltschemata ist ANPC in der Lage, die schnell schaltenden Bauelemente auf SiC-MOSFETs und die langsam schaltenden Bauelemente auf Si-IGBTs zu verlagern. Auf diese Weise werden die Schaltverluste bei hoher Schaltfrequenz stark reduziert. Die Lösung ist nicht neu für Anwendungen mit geringem Stromverbrauch, bei denen alle Schalter als diskrete Bauelemente auf einer kleinen Leiterplatte verbunden sind oder alle Schalter in ein Modul integriert sind, das geringe Induktivitäten in den Kommutierungsschleifen aufweist. Bei Anwendungen mit hoher Leistung besteht die größte Herausforderung des Konzepts in den hohen Induktivitäten der Kommutierungsschleifen, die die Schaltgeschwindigkeit der Geräte begrenzen. Es gibt zwei Arten von hybriden ANPC, die sich durch die Anzahl der verwendeten SiC-MOSFETs unterscheiden: 4SiC- und 2SiC-Hybrid-ANPC. Die 4SiC-Version wird aufgrund der kleinen Kommutierungsschleifen der Hochgeschwindigkeits-SiC-MOSFETs für Hochleistungsanwendungen bevorzugt. Der 2SiC-Hybrid-ANPC hingegen kann wegen der langen Kommutierungsschleifen seiner MOSFETs nicht für Hochleistungsanwendungen eingesetzt werden. Die langen Kommutierungsschleifen können zwar durch einen Entkopplungskondensator in der Nähe des SiC-MOSFET entkoppelt werden. Aber das Vorhandensein des Entkopplungskondensators in der 2SiC-Hybrid-ANPC-Topologie für hohe Leistungen stellt viele Herausforderungen im Designprozess und in der praktischen Umsetzung dar. Diese Dissertation befasst sich mit den Problemen, die für diese Topologie besonders wichtig sind. Darüber hinaus stellt die Entwicklung eines Hochgeschwindigkeits-Schalt-MOSFETs eine eigene Reihe von Herausforderungen dar. Einige neuartige und interessante Lösungen für diese Probleme werden in dieser Dissertation ebenfalls vorgeschlagen. Ein experimenteller 500 kW 2SiC-Hybrid-ANPC wird gebaut, um diese Konzepte zu beweisen.

Contents

List of Acronyms

3L-ANPC: Three-level active neutral point clamped

3L-TDANPC: Three-level two-stage decoupled active neutral point clamped

AC: Alternating current

ACL: Active clamping

ADC: Analog-to-digital converter

AGD: Active gate driver

AISI: American Iron and Steel Institute

BW: Band width

CAN: Controller area network

DC: Direct current

DSP: Digital signal processor

EMI: Electromagnetic interference

EMC: Electromagnetic compatibility

EN: European Standard

ESL: Equivalent series inductance

ESR: Equivalent series resistance

FR: Ferrite core

FPGA: Field programmable gate arrays

HF: High frequency

IGBT: Insulated-gate bipolar transistor

LF: Low frequency

MOSFET: Metal oxide semiconductor field effect transistor

PCB: Printed circuit board

PTO: Parasitic turn-on

PWM: Pulse width modulation

RMS: Root mean square

Si: Silicon

SiC: Silicon Carbide

SOA: Safe operating area

THD: Total harmonic distortion

TIM: Thermal interface material

TVS: Transient voltage suppressor

WIFI: Wireless fidelity

List of Figures

List of Tables

1. Introduction

The growing demand for renewable energy has resulted in an increased demand for grid-tied inverters with low output current harmonics [1, 2, 5]. Achieving low output current harmonics typically involves a passive L, LC, or LCL filter at the inverter's output. However, these filters, particularly the inductors, often occupy a significant portion of the entire inverter's volume. In numerous applications, the need to minimize the size of the passive filter stands out as a crucial requirement. As the dimensions of the inductors become more critical, a shift from the conventional 2-level topology to a multilevel topology and higher switching frequencies becomes necessary. This adjustment aims to reduce the output current ripple and consequently shrink the volume of the filter inductor [23].

1.1 Filter inductor's volume

If we assume that the inductor's volume is directly proportional to its stored energy, the volume of the inductor can be calculated by (1.1) [3].

$$V_L = k_L L \cdot I^2 \tag{1.1}$$

With L and I are the inductance and nominal current of the inductor, k_L is volume coefficient of the inductor, which depends on average volume of the core magnetic material, V_L is the volume of the inductor.

In high power system, LCL, LC filter is normally preferred instead of L filter because of its low cost and high frequency attenuation capability [1, 5]. For 2-level inverter, minimum value required for the inverter side inductor (L_{I2}) according to [4] is:

$$L_{I2} = \frac{V_{DC}}{6 \cdot f_{sw} \cdot \Delta I_{max}} \tag{1.2}$$

In case of 3-level inverter, minimum value required for the inverter side inductor (L_{I3}) according to [5] is:

$$L_{I3} = \frac{V_{DC}}{16 \cdot f_{sw} \cdot \Delta I_{max}} \tag{1.3}$$

In which, f_{sw} is the switching frequency of the inverter, ΔI_{max} is the maximum allow output current ripple.

From equations (1.2), (1.3), at the same maximum output current ripple, DC link voltage and switching frequency, 3-level inverter can reduce the inductance 2.5 times compare to 2-level topology at the same switching frequency and hence reduce the volume of the passive filter. The volume of the inductor can be further reduced by increasing the switching frequency. Therefore, SiC MOSFET is an attractive solution in this scenario.

Table 1.1: *PLECS simulation parameters*.

Grid line-line voltage	V_g	690V
Nominal RMS current	I_n	300A
Transformer short-circuit impedance	u_k	5%
DC link voltage	V_{DC}	1500V
Maximum current ripple	ΔI_{max}	50A
Grid side inductance	L_g	211µH
2-level switching frequency	f_{s2}	2.5kHz
3-level switching frequency	f_{s3}	10kHz
2-level inverter side inductance	L_{I2}	2mH
3-level inverter side inductance	L_{I3}	188µH

To illustrate the benefits of high switching frequency and a 3-level inverter over a conventional 2-level inverter for minimizing the size of the filter's inductor, a PLECS

simulation is setup like in Figure 1.1a and Figure 1.2a. The simulation parameters are shown in Table 1.1.

The filter inductor for 2-level L_{I2} and 3-level L_{I3} are determined using equations (1.2) and (1.3), with a maximum current ripple ΔI_{max} of 50A. The 2-level inverter operates at 2.5kHz switching frequency while the 3-level inverter is switched at 10kHz.

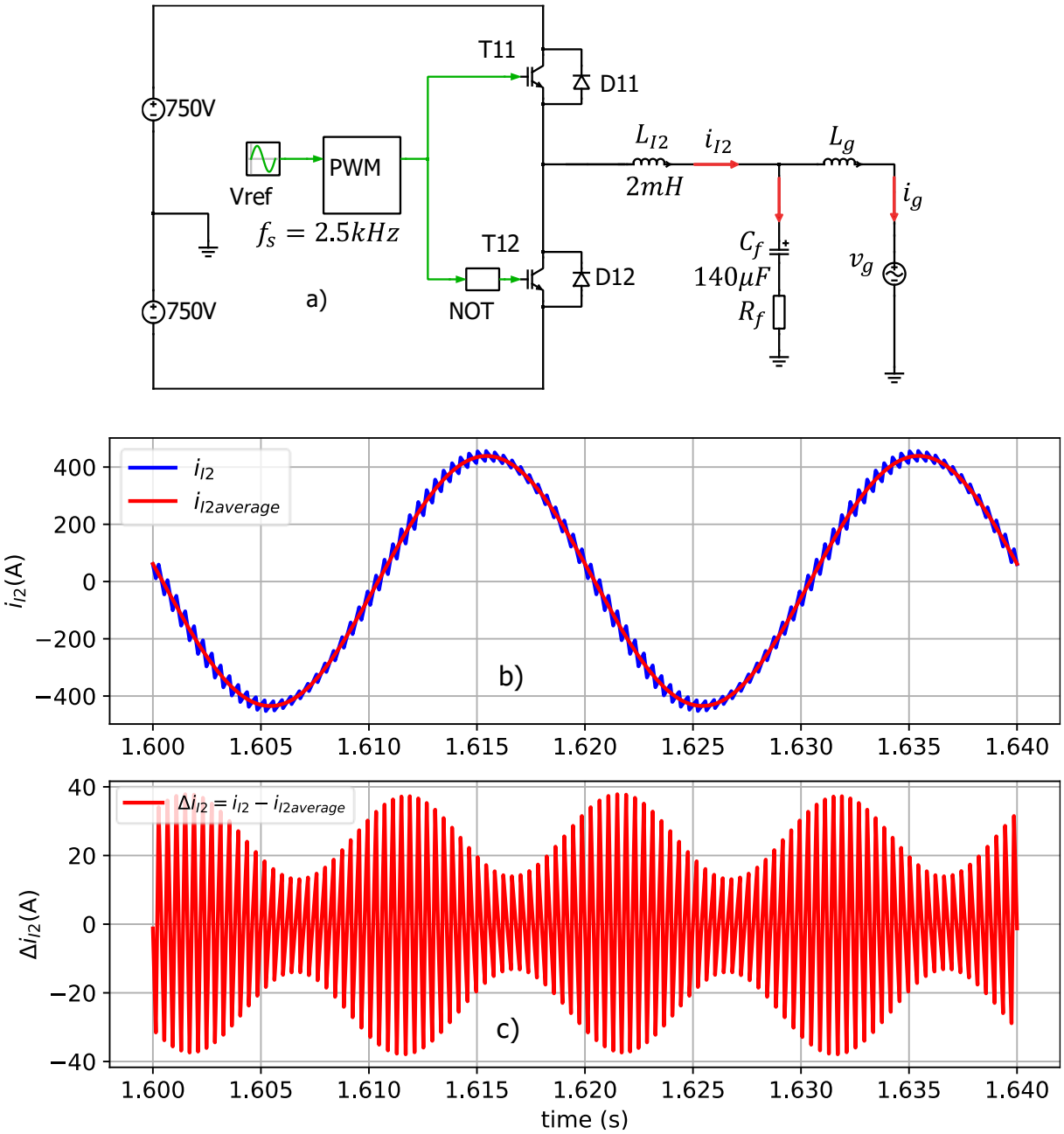


Figure 1.1: *PLECS simulation: a) 2-level inverter f_{s2}= 2.5kHz, b) Output current before the LC filter and its average value, c) peak to peak current ripple.*

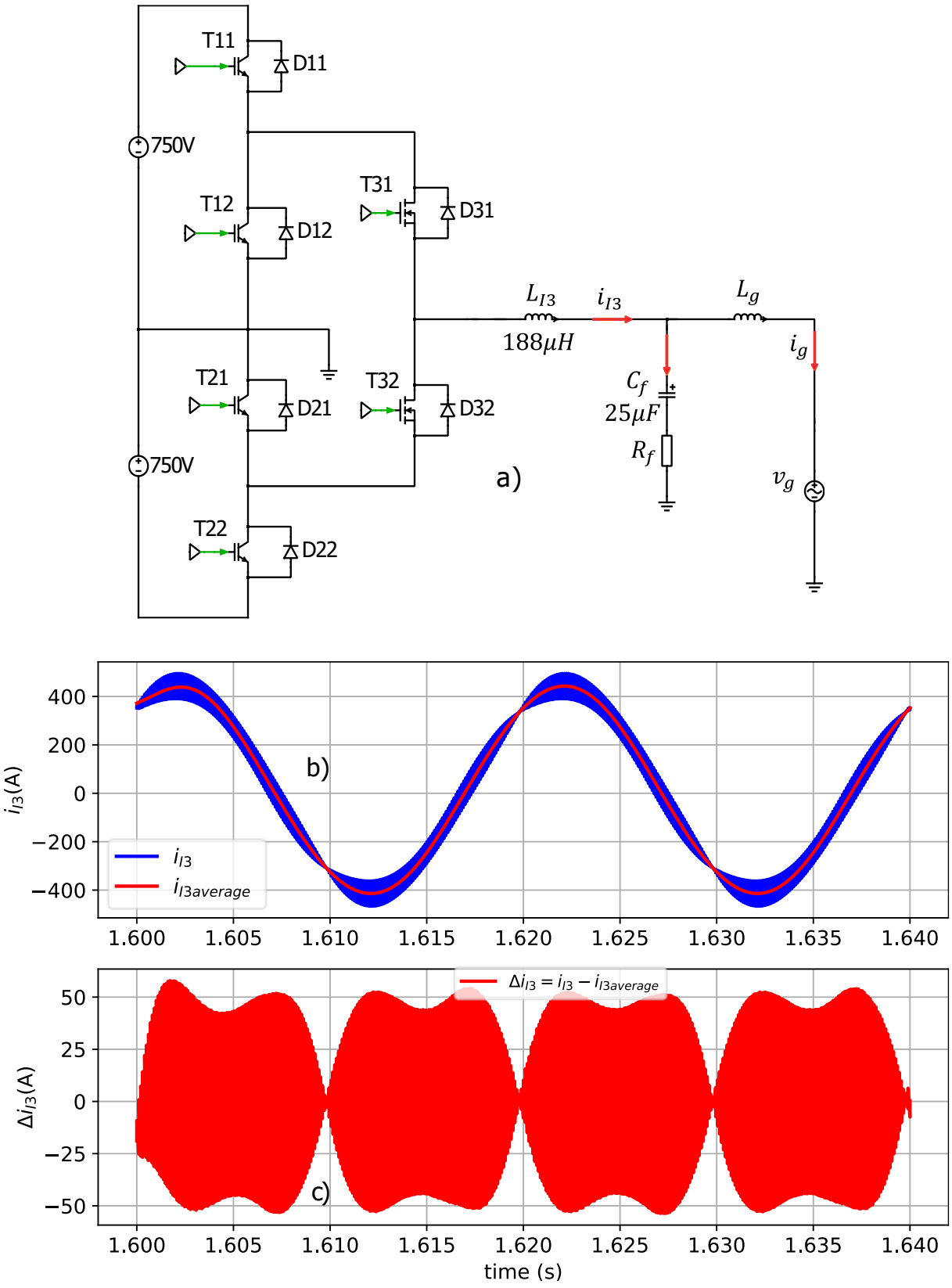


Figure 1.2: *PLECS simulation: a) 3-level inverter f_{s3}= 10kHz, b) Output current before the LC filter and its average value, c) peak to peak current ripple.*

Assuming the line to line grid voltage V_g of 690V and considering a transformer with a short-circuit impedance u_k of 5%, a rated current $I_n$of 300Arms, its equivalent inductance can be determined as $L_g = 211\mu H$. It is assumed that the transformer's resistance is neglectable. The peak to peak ripple of the output current for the 2-level inverter is depicted in Figure 1.1c while that of the 3-level inverter is shown in Figure 1.2c. The peak-to-peak ripple is determined by subtracting the average inverter current from the inverter output current. It's important to highlight that the average current, being sinusoidal and in phase with the inverter output current. This subtraction yields the actual peak-to-peak ripple. However, the grid current, despite being sinusoidal, undergoes phase shifting due to the LC filter. Subtracting it from the inverter current will not accurately reflect the true ripple.

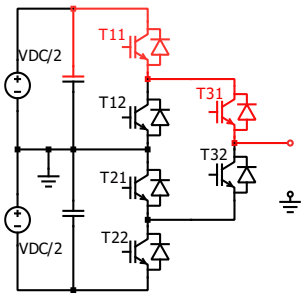
Despite both cases has current ripple of approximately 50A, the 2-level filter's inductor is 10 times larger than the 3-level filter's inductor.

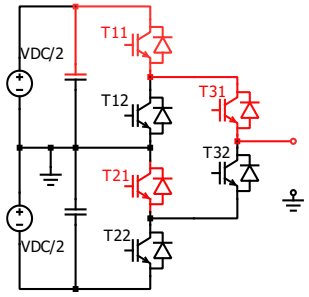
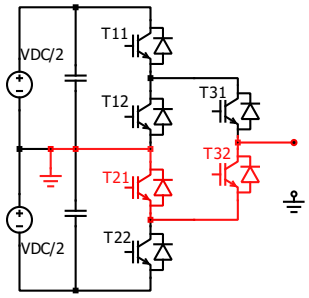
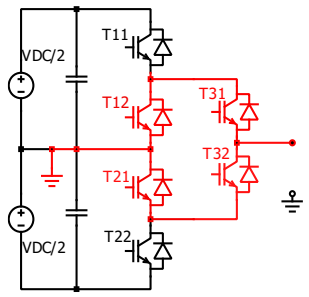
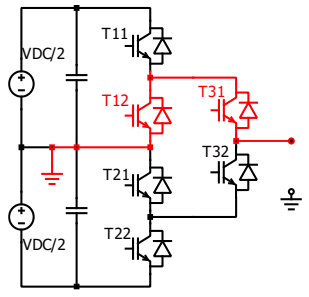
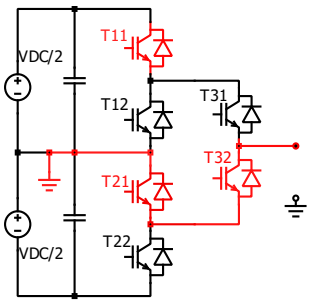
1.2 Three-level active neutral point clamp (3L-ANPC)

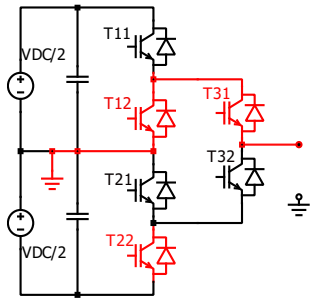
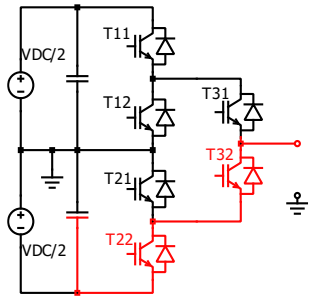
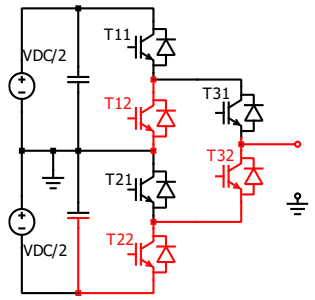
1.2.1 ANPC switching states

ANPC is famous for its flexible losses distribution since it was first introduced [6]. The flexibility comes from its variety of switching states which can be seen in Table 1.2.

Table 1.2: *ANPC's different switching states.*

State	V_{out}	T11	T12	T21	T22	T31	T32	
P1	$\frac{V_{DC}}{2}$	1	0	0	0	1	0	

P2	$\frac{V_{DC}}{2}$	1	0	1	0	1	0	
Z1	0V	0	0	1	0	0	1	
Z2	0V	0	1	1	0	1	1	
Z3	0V	0	1	0	0	1	0	
Z4	0V	1	0	1	0	0	1	

Z5	0V	0	1	0	1	1	0	
N1	$-\frac{V_{DC}}{2}$	0	0	0	1	0	1	
N2	$-\frac{V_{DC}}{2}$	0	1	0	1	0	1	

1.2.2 ANPC's flexible pulse width modulation (PWM) strategies

Table 1.3: *PWM-1 [16].*

States	T11	T12	T21	T22	T31	T32	Note
P=P1	1	0	0	0	1	0	Switching cycle: $V_{out} \geq 0$: P-ZP-P, $V_{out} \leq 0$: N-ZN-N. T11, T12, T21, T22 are switched at f_s in ½ fundamental cycle T31, T32 are switched at f_0
ZP=Z3	0	1	0	0	1	0	
ZN=Z2	0	0	1	0	0	1	
N=N1	0	0	0	1	0	1	

Table 1.4: *PWM-2 [13].*

States	T11	T12	T21	T22	T31	T32	
P=P2	1	0	1	0	1	0	Switching cycle: $V_{out} \geq 0$: P-ZP-P, $V_{out} \leq 0$: N-ZN-N. T11, T12, T21, T22 are switched at f_0. T31, T32 are switched at f_s in a full fundamental cycle
ZP=Z4	1	0	1	0	0	1	
ZN = Z5	0	1	0	1	1	0	
N = N2	0	1	0	1	0	1	

Table 1.5: *PWM-3 [14].*

States	T11	T12	T21	T22	T31	T32	
P = P2	1	0	1	0	1	0	Switching cycle: $V_{out} \geq 0$: P-ZP1-P-ZP2-P, $V_{out} \leq 0$: N-ZN1-N-ZN2-N T11, T12, T21, T22 are switched at f_s in ½ fundamental cycle T31, T32 are switched are switched at f_s in full fundamental cycle.
ZP1=Z3	0	1	0	0	1	0	
ZP2=Z4	1	0	1	0	0	1	
ZN2=Z5	0	1	0	1	1	0	
ZN1=Z1	0	0	1	0	0	1	
N=N2	0	1	0	1	0	1	

Table 1.6: *PWM-4 [10].*

States	T11	T12	T21	T22	T31	T32	
P=P2	1	0	1	0	1	0	Switching cycle: $V_{out} \geq 0$:P-Z-P, $V_{out} \leq 0$:N-Z-N T11, T12, T21, T22, T31, T32 are switched at f_s in ½ fundamental cycle
Z=Z2	0	1	1	0	1	1	
N=N2	0	1	0	1	0	1	

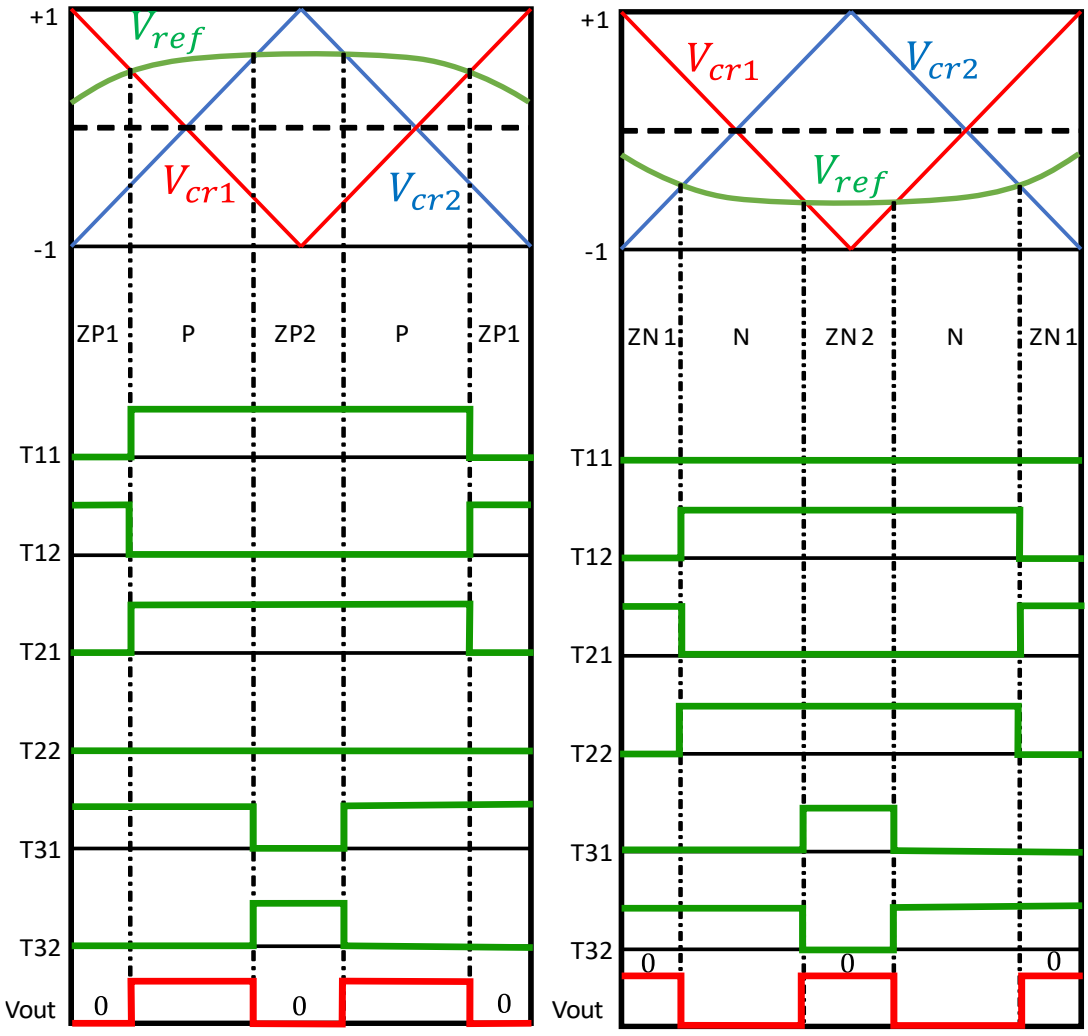


Figure 1.3: *PWM-3 switching pattern. V_{out} has apparently double the switching frequency [14].*

There are many different PWM strategies for ANPC have been published in literature [6-14]. They used different combinations of those above switching states to flexibly assign the high switching frequency on different switches. By doing so, the switching losses can be flexibly distributed among the switches.

In PWM-1 (Table 1.3), T11, T12, T21, T22 are switched at switching frequency f_s in a haft of fundamental cycle (orange color), T31, T32 are switched at fundamental frequency f_0 (green color). Most of the switching losses are located on T11, T12, T21, T22.

In PWM-2 (Table 1.4), T11, T12, T21, T22 are switched at fundamental frequency f_0 (green color), while those switches T31, T32 are switched at switching frequency f_s in a full fundamental cycle (yellow color). Most of the switching losses are located on T31, T32.

In PWM-3 (Table 1.5), the two carriers V_{cr1}, V_{cr2} are on the same axis with 180° phase shifted. The switching patterns are shown in Figure 1.3. V_{cr1}, V_{cr2} have the frequency f_s, but the output voltage is apparently switched $2xf_s$ [14]. T12, T21 are switched at f_s in a full fundamental cycle, but in half of the cycle, they commutate without load current (orange color). T11, T22 are switched at f_s in a half of fundamental cycle (orange color). T31, T32 are switched at f_s in a full fundamental cycle (yellow color).

In PWM-4 (Table 1.6) uses only Z2 for its zero state, in which, 4 switches T12, T21, T31, T32 are on. The neutral state shares the load current to both upper and lower neutral path. Thus, the conduction loss on each switch is lower in compare with the other PWM strategies. But the disadvantage is that, all six switches are switched at the switching frequency f_s in a half of fundamental cycle.

1.2.3 ANPC's different commutation loops

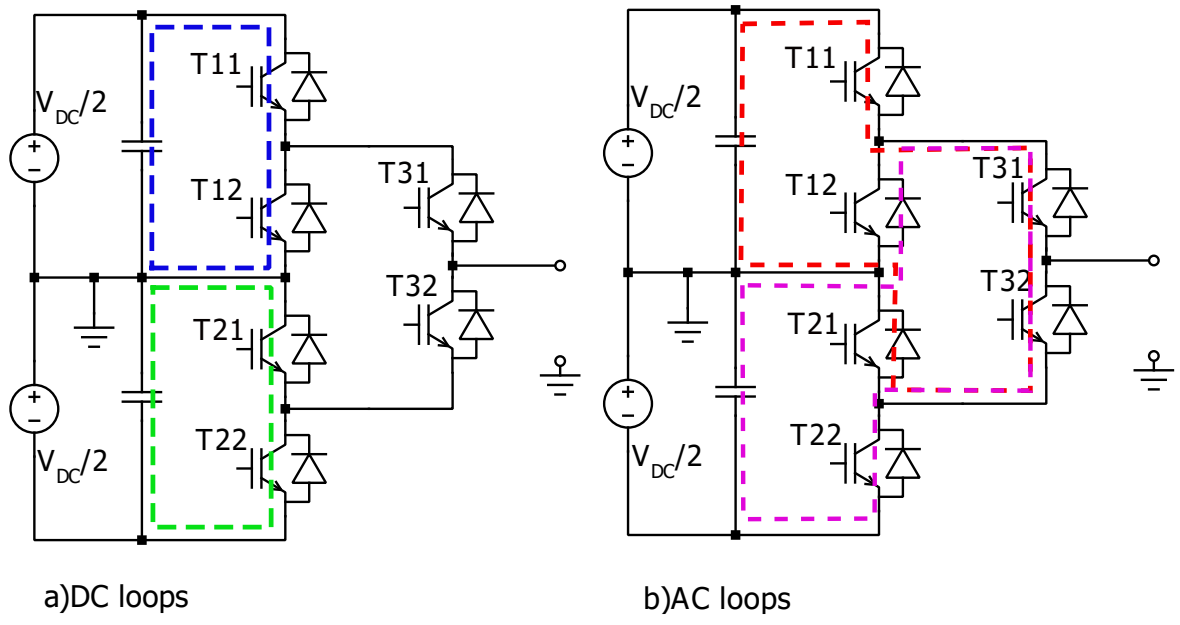


Figure 1.4: *3-Level Active neutral point clamped (ANPC) topology and its commutation loops. a) T11, T12, T21, T22's commutation loops: dashed blue, green lines. b) T31, T32's commutation loops: red, pink dashed lines.*

Each switch in the ANPC has its own commutation loop, which depends on the actual switching state and the load current's location. In Figure 1.4, T11, T12 have the same commutation loop (blue dashed line), T21, T22 have the same commutation loop (green dashed line). T31, T32 have the same commutation loop (red dashed line) when the load current is on the upper side of the ANPC or the pink dashed line when the load current is on the lower side of the ANPC. If it is assumed that the layout of the inverter is symmetrical, T11, T12, T21, T22 have equal commutation loop and it is called DC loop, T31, T32's commutation loops are equal and it is called AC loop. Because T11, T12, T21, T22 are closed to the DC link capacitor than T31, T32, the DC loop has smaller inductance than the AC loop.

1.3 Hybrid Si/SiC ANPC

The flexible losses distribution of ANPC is the inspiration for many publications about hybrid ANPC topologies [15-21, 26, 27], in which, the high-speed Si IGBT switches will be replaced with SiC MOSFETs. Those publications can be divided into two main streams: one is replacing 4 Si IGBTs T11, T12, T21, T22 with four SiC MOSFETs [15, 16, 20] (Figure 1.5a), this can be called 4SiC hybrid ANPC, the topology uses switching schemes PWM-1 to relocate the high-speed switches on four SiC MOSFETs which have short DC commutation loops. The other main stream is replacing two Si IGBTs T31, T32 with two SiC MOSFETs [16, 17, 18, 19, 21, 22, 26, 27] (Figure 1.5b, c), this can be called 2SiC hybrid ANPC, this topology uses switching scheme PWM-2 to relocate the high-speed switches on two SiC MOSFETs which have long AC commutation loops.

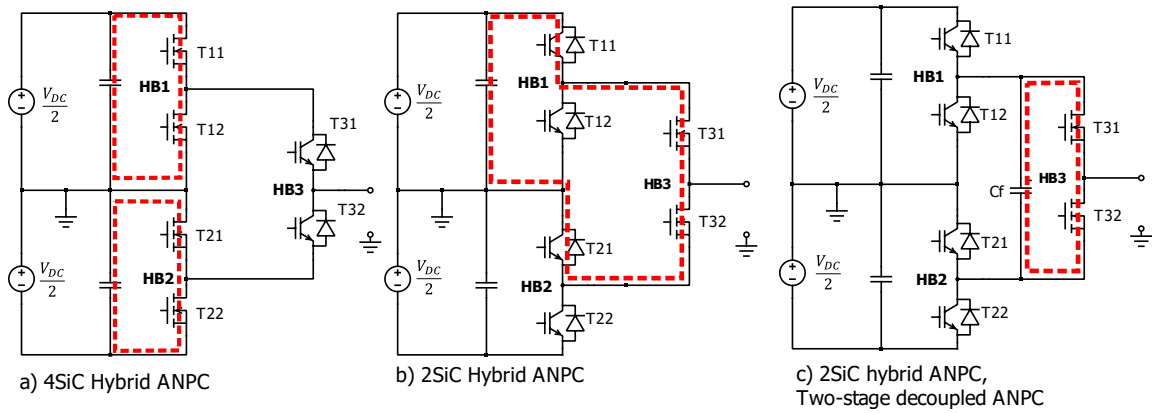


Figure 1.5: *Hybrid ANPC topology, a) 4SiC-Hybrid ANPC [15], b) 2SiC-Hybrid ANPC [21], c) Two-stage decoupled ANPC (3L-TDANPC) [26].*

The majority of publications have concentrated on low-power applications, achievable through the use of discrete SiC chips on a printed circuit board [16-19], or by integrating all switches into a single module [21] (refer to Table 1.7). In these configurations, the difference between DC loops' inductances and AC loops' inductances are small, 2SiC or 4SiC hybrid ANPC can be implemented without constraints. In contrast, high-power applications involve separate high-power modules, connected by a busbar [15, 20, 26, 27]. This setup significantly raises the inductances of the commutation loops. In those setups, the differences between the DC loops and AC loops inductance are large. Therefore, 4SiC hybrid ANPC is more attractive than 2SiC hybrid ANPC due to its shorter DC commutation loops. As it can be seen in [15], a 4SiC hybrid ANPC in megawatt scaled was introduced. But the high cost due to 4 SiC MOSFETs is a major disadvantage of this topology.

Table 1.7: *Overview of publication on hybrid Si/SiC ANPC.*

Article	Output power	Power switches	Topology	Note
[15, 20]	1MW	Half-bridge modules	4SiC	busbar
[16]	2kW	Discrete chips	4SiC/2SiC	Chips on PCB
[17]	1kW	Discrete chips	2SiC	Chips on PCB
[18]	3.3kW	Discrete chips	2SiC	Chips on PCB
[19]	Not defined	Discrete chips	2SiC	Chips on PCB
[21]	116kW	Integrated module	2SiC	Integrated module
[26, 27]	1MW	Half-bridge modules	2SiC 3L-TDANPC	busbar

The 2SiC hybrid ANPC can be implemented for high power applications with help of a decoupling capacitor C_f like Figure 1.5c. In which, the decoupling capacitor shorten the MOSFETs' commutation loops. Di Zhang has introduced one 1MW inverter of this topology

in [26, 27] which is called two-stage decoupled ANPC (3L-TDANPC). The 3L-TDANPC has the advantage of low number SiC MOSFETs are used but it also introduces the low frequency resonance in the busbar circuit because of decoupling capacitor. The low frequency resonance raises the concern about the electromagnetic interference (EMI) and electromagnetic compatibility (EMC) and it is need to be damped during the operation [26].

1.4 The motivation and challenges of this dissertation

One biggest challenge for high power three-level hybrid ANPC is the large commutation loop's inductance due to its complex busbar structure [15]. Especially, the MOSFETs in 2SiC hybrid ANPC have the longest commutation loop. Switching those MOSFET at high speed is unpractical without the decoupling capacitor. Adding the decoupling capacitor actually introduces a complex high order circuit which includes the IGBTs and MOSFETs in its loops. The complex equivalent circuit of the hybrid ANPC can be seen in Figure 1.6. Finding the analytical solutions for this type of circuit under different operating conditions is difficult. Moreover, having the analytical model of the circuit is essential for a successful design of the 2SiC hybrid ANPC because it can provide information about the circuit's boundary and components' limit, which is a reference for component selection. The topology was first introduced in [26], but no analytical solution was provided. Especially when the inverter is operated under unbalanced DC link voltage [24, 25].

Apart from that, the decoupling capacitor forms a low frequency resonance circuit between the busbar's inductance and the decoupling capacitor, which poses an EMI risk for the inverter's system [26]. Not many effective solutions for damping this resonance has been published. D.Zhang proposed the gate-off active damping scheme in [26], can address this issue, but its dependence on the load current direction makes the method less attractive for realistic implementation

Those challenges above are very specified for this topology. Apart from that, designing a high-speed switching SiC MOSFET has some common challenges like the high frequency ringing [33-34] or snappy body diode's reverse-recovery [104, 29, 30]. The overvoltage and oscillation on the body diode during the reverse-recovery has a strong impact on the turn-on speed of the MOSFET in a half-bridge module. It depends not only on the chip technology but also the external circuitry and driving conditions [104]. Understanding the relationship between

the diode's behavior and the reverse-recovery overvoltage, oscillation is necessary for the optimization of the turn-on losses and overvoltage protection. Unfortunately, there is no publication focus on modeling both the reverse-recovery overvoltage and oscillation especially in transient states. Moreover, SiC MOSFET has some well-known issues with the threshold voltage instability, or changing with temperature and aging effect [106, 107, 108, 109, 110]. The characterization process of the MOSFET should take those effects into consideration.

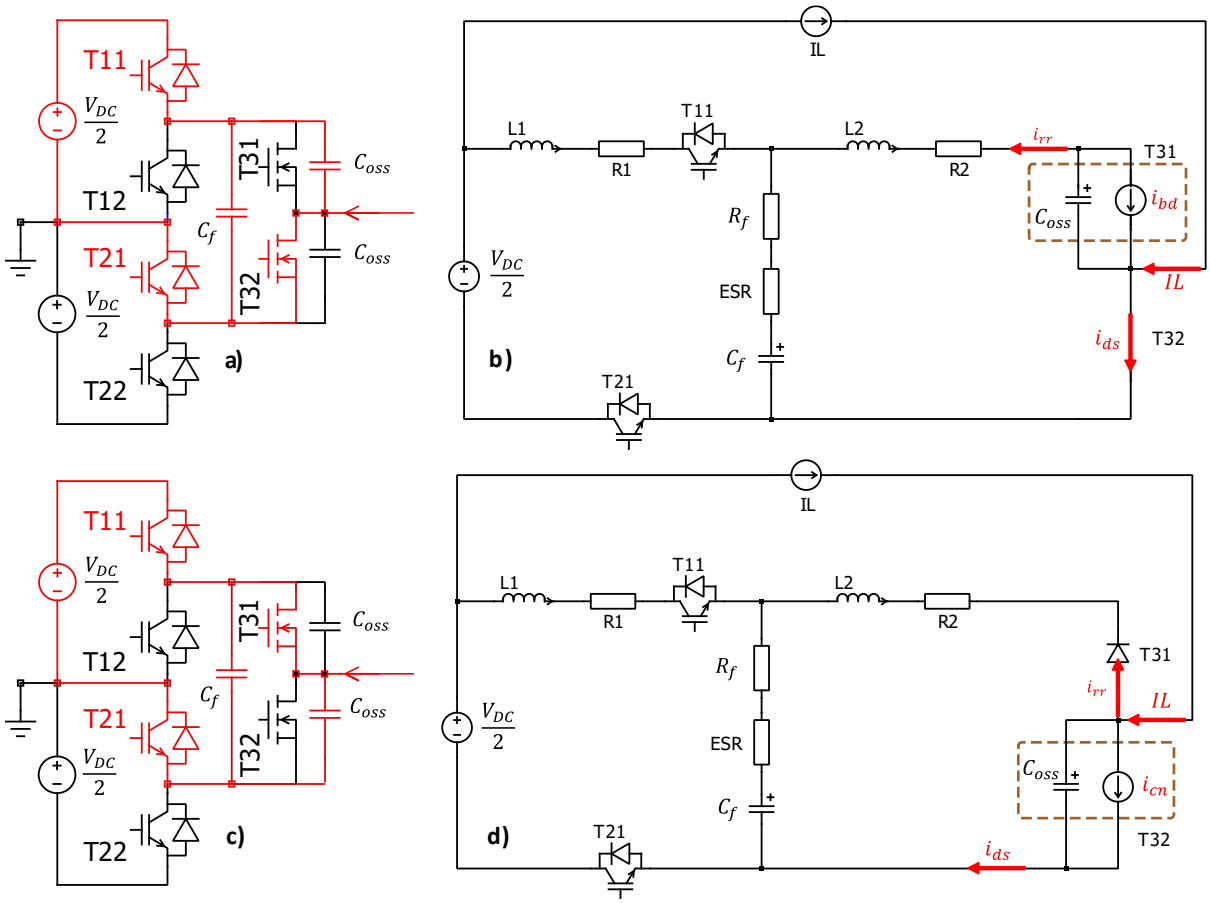


Figure 1.6: *2SiC hybrid ANPC with decoupling capacitor a) when T32 is on, c) when T32 is off, b, d) The equivalent circuit of those 2 cases.*

1.5 New contributions from this dissertation

1. The operation of the 3-level two stages decouple ANPC under unbalanced DC link voltage is investigated.
2. Damping the high switching frequency oscillations of SiC MOSFET using the skin effect capacitor.

3. Explore the new potential of using ferrite cores for effectively damping the high switching oscillation of SiC MOSFET.
4. New single pulse method to measure the core's differential inductance in deep saturation region.
5. Introduced the new switching scheme for the two stages decouple ANPC which effectively cuts off the low frequency oscillation and independent from the load current.
6. Modeling the reverse-recovery oscillation and overvoltage of SiC MOSFET which unveils the mechanism behind the phenomenon.
7. Discover the ability to utilize the active clamping to protect the SiC MOSFET from both turn-off and reverse-recovery overvoltage.

The organization of this dissertation:

Chapter 2 explains the coupled oscillations in the 2SiC hybrid ANPC. The effect of unbalanced DC link voltage on the inverter operation is described. Some basic knowledges about the resonance circuits used in this chapter are provided in the appendix 1.

Chapter 3 of the dissertation explores some interesting techniques to effectively dampen the native SiC MOSFET's ringing, including the skin effect of a special stainless-steel material and the installation of a dual soft ferrite cores directly on the power loop.

Chapter 4 introduces the active cut-off switching scheme and the optimization of the switching transition timing.

Chapter 5 describes the modeling of the reverse-recovery oscillation and overvoltage. Moreover, this chapter also presents a possibility to utilize the active clamping to protect the SiC MOSFET from both turn-off and reverse-recovery overvoltage.

To validate those proof of concepts, a 500kW 3L-TDANPC has been designed with parameters outlined in Table 1.8. Appendix2 provides details of both the hardware and software design aspects of this inverter.

Chapter 6 provides the information about the characterization of SiC MOSFETs and IGBTs in this 2SiC ANPC. One phase of the inverter was setup to run continuously at rated

current for 2 hours to verified the temperature limit of the inverter's critical components. The results are discussed. The performance of 4SiC ANPC and 2SiC ANPC are also compared in this chapter.

Chapter 7 concludes with a summary of key findings and insights drawn from the research. Additionally, future research directions and potential areas for further exploration within this topic are outlined.

Table 1.8: *500kW 3L-TDANPC parameters.*

Parameters	Value
Output power	520kVA/500kW
DClink voltage	1500V
Output voltage	3phases, 50 Hz, V_{LL} = 1000V
Output current	300Arms
Switching frequency	10kHz
Cooling method	Forced air cooling

2. Switching Oscillations In a 2SiC Hybrid ANPC

2.1 Equivalent oscillation circuits of a 2SiC hybrid ANPC

Since the ANPC exhibits symmetrical characteristics between its upper and lower sides, it is possible to investigate the switching oscillations on the upper side, which mirror those occurring on the lower side. In the conventional switching arrangement, during the inverter's transition between P and ZP states, T11 and T21 remain consistently on, while T31 and T32 switch on and off at the switching frequency. Assuming symmetry between T31 and T32, the switching oscillations happen at T32's turn-on and turn-off are similar to T31's.

Figure 2.1a present the oscillation circuit in the ANPC during T32's turn-on. When T32's is fully conducting, T31's body diode enters the reverse-recovery process. Its current slope i_{bd} at the end of the reverse-recovery process triggers both high frequency and low frequency oscillation circuits. The high frequency oscillation circuit is formed by T31's output capacitor C_{oss} and the small commutation loop inductance L_2between the decoupling capacitor C_f and C_{oss}. The low frequency oscillation circuit consists of the decoupling capacitor C_f and the large commutation loop inductance between the DC link capacitors and C_f. The equivalent circuit can be seen in Figure 2.1b.

Similarly, when T32 is turned off, T32's channel current slope i_{cn} triggers both high and low frequency oscillation circuits. The high and low frequency oscillation circuits are similar to the first case when T32 is turned on. But the output capacitor in this case is T32's C_{oss} (Figure 2.1d). Since the output capacitors of T31 and T32 are equal, their oscillation circuits are similar like Figure 2.1e. The only difference is the current slope i_{slope}. When T32 is on, i_{slope} is the body diode's current i_{bd}. When T32 is off, i_{slope} is T32's channel current i_{cn}.

The oscillation circuit in Figure 2.1e is a coupled LCR network: L_1C_f $(R_1 + ESR + R_f)$ and L_2C_{oss} $(R_2 + ESR + R_f)$ which ESR, R_f are the internal and external resistance of the decoupling capacitor. When C_f satisfies the decoupling conditions, the circuit is effectively split into two distinct frequency loops: the low-frequency loop (depicted as the blue dashed line, labeled LF) and the high-frequency loop (represented by the red dashed line, labeled HF).

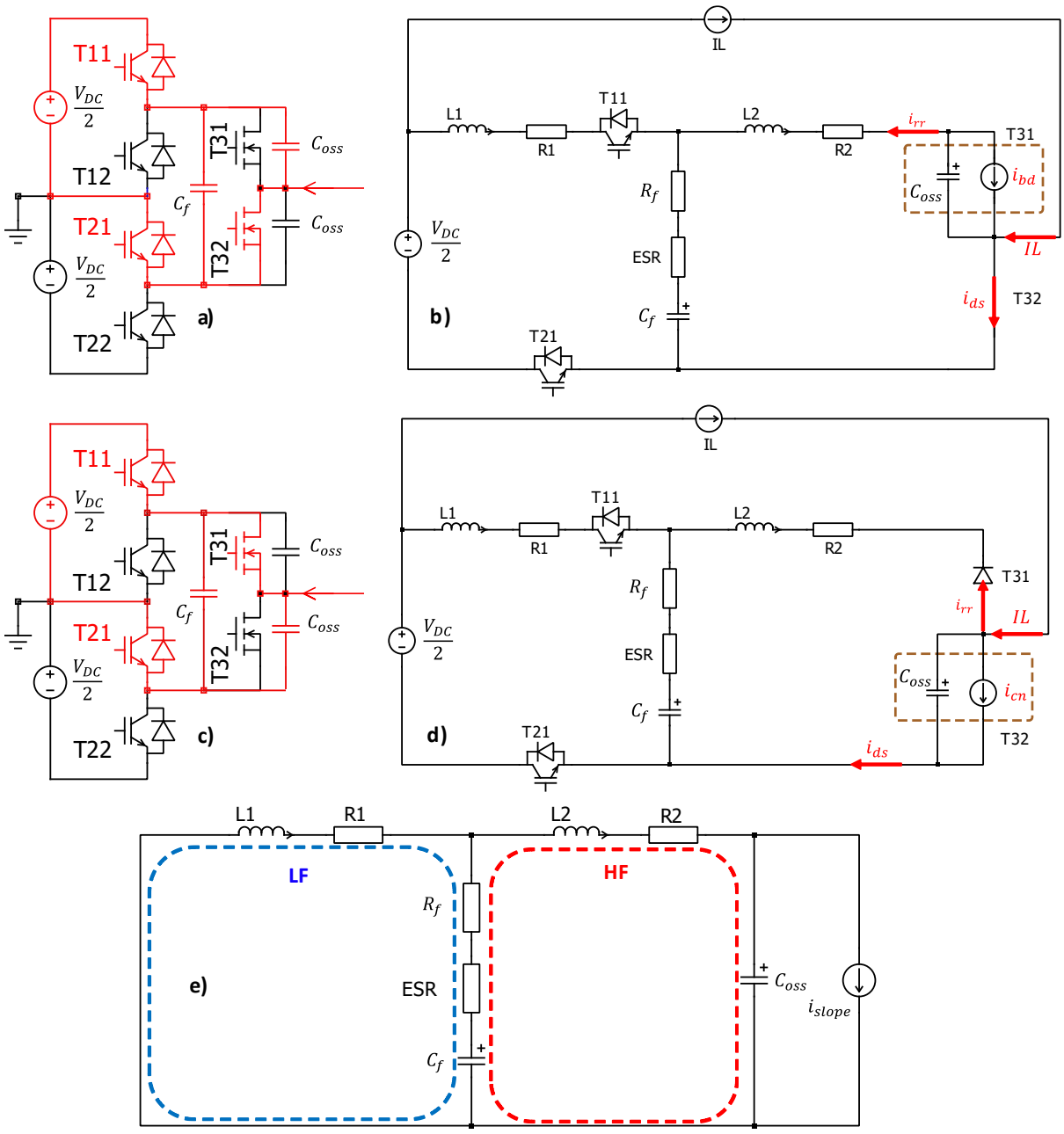


Figure 2.1: *Oscillation circuits in ANPC when a) T32 is turned on, b) Equivalent circuit when T31's body diode is in its reverse-recovery, c) T32 is turned off, d) Equivalent circuit during T32's turn-off e) The small AC signal equivalent circuit during T32's turn-on and turn-off*

2.1.1 Low frequency loop (LF)

Notably, the LF resonance current can circulate in LF circuit in both directions because of the on state IGBTs T11, T21 and diodes D11, D21. If one of the IGBTs is turned off, the resonance current can flow only in one direction. The cycle of exchange energy between the inductor and capacitor is broken down and the oscillation is cut off. Because the LF circuit consists a $V_{DC}/2$ voltage source, the value of the initial voltage of the decoupling capacitor (V_{cf0}) compared to $V_{DC}/2$ will decide the LF's amplitude. If all the resistances are small and neglectable, the voltage and current of the decoupling capacitor are:

$$i_{cf}(t) = I_L \cdot \cos(\omega_1 t) - \frac{V_{cf0} - \frac{V_{DC}}{2}}{\sqrt{\frac{L_1}{C_f}}} \cdot \sin(\omega_1 t) \quad (2.1)$$

$$v_{cf}(\omega_1 t) = I_L \cdot \sqrt{\frac{L_1}{C_f}} \cdot \sin(\omega_1 t) + (V_{cf0} - V_{DC}/2) \cdot \cos(\omega_1 t) + V_{DC}/2 \quad (2.2)$$

$$\omega_1 = 1/\sqrt{L_1 C_f} \quad (2.3)$$

Equation (2.2) shows the maximum voltage of the decoupling capacitor is:

$$V_{cfmax} = \sqrt{I_{Lmax}^2 \cdot \frac{L_1}{C_f} + \left(V_{cf0} - \frac{V_{DC_{max}}}{2}\right)^2} + V_{DC_{max}}/2 \quad (2.4)$$

If the decoupling capacitor is discharged to zero during switching or $V_{cf0} = 0$, V_{cfmax} reaches its critical value at:

$$V_{cfmax} = \sqrt{I_{Lmax}^2 \cdot \frac{L_1}{C_f} + \frac{V_{DC_{max}}^2}{4}} + V_{DC_{max}}/2 \quad (2.5)$$

This means keeping the voltage of the decoupling capacitor constant at $V_{DC}/2$ is critical to avoid overvoltage on the MOSFET during the switching. Therefore, at the start-up of the

inverter, the decoupling capacitor should be charged to $V_{DC}/2$ before the switching is enable. From the equation (2.1), at the start-up of the inverter, $V_{cf0} = 0$ and IL = 0, the capacitor charging current is:

$$i_{cf}(t) = \frac{V_{DC}}{2 \cdot \sqrt{\frac{L_1}{C_f}}} \cdot \sin(\omega_1 t) \qquad (2.6)$$

The larger C_f is, the higher the peak current is, which can be seen in Figure 2.2. The charging current is handled by the IGBTs, consequently, the value of the decoupling capacitor should be limited to a maximum value so that the peak charging current is under the IGBT's maximum repetitive collector current (I_{CRM}). The high initial charging current can be avoided by a proper start-up sequence: T11, T21 are on first and then increasing DC link voltage slowly to the operating voltage.

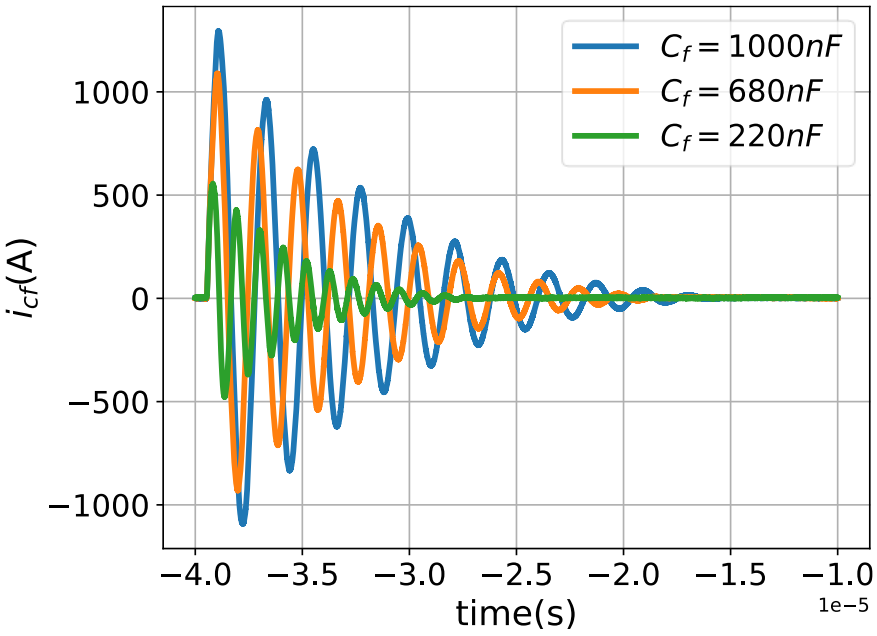


Figure 2.2: *Different capacitor charging current at start-up of the ANPC at 1000 V_{DC}, C_f = 1000nF, 680nF and 220nF.*

2.1.2 High frequency loop (HF)

At the MOSFET's turn-off, the channel current transient triggers the HF oscillation. The small signal equivalent circuit of the HF loop is shown in Figure 2.3. Assumed that the

MOSFET's output capacitor is constant during the turn-off transient. The turn-off channel current can be model as:

$$i_{cn}(t) = IL + at \tag{2.7}$$

With a is the turn-off current slope.

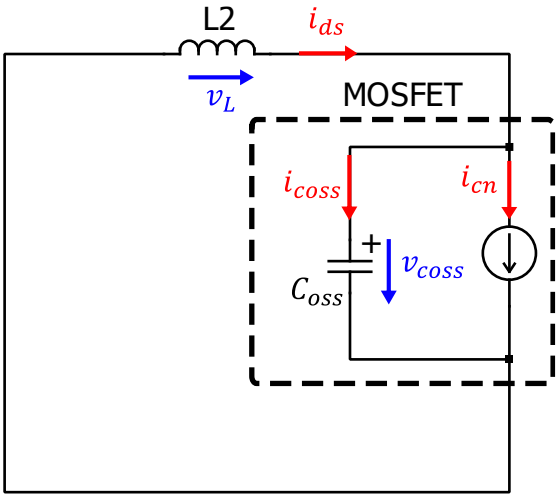


Figure 2.3: *The small signal circuit of the high frequency oscillation circuit (HF) during MOSFET's turn-off current transient.*

$$i_{cn}(t) + i_{coss}(t) = i_{ds}(t) \tag{2.8}$$

$$v_L(t) = L_2 \frac{di_{ds}}{dt} = -v_{coss}(t) \tag{2.9}$$

$$i_{coss}(t) = C_{oss} \frac{dv_{coss}}{dt} \tag{2.10}$$

Take derivative 2 sides of (2.8):

$$\frac{di_{cn}}{dt} - \frac{di_{ds}}{dt} + \frac{di_{coss}}{dt} = 0 \tag{2.11}$$

Take derivative of (2.10), (2.7) and replace to (2.11):

$$C_{oss} \cdot v''_{coss} + \frac{1}{L_2} \cdot v_{coss} + a = 0 \tag{2.12}$$

Solve (2.12), the general solution is:

$$v_{coss}(t) = A_1 \sin(\omega_2 t) + A_2 \cos(\omega_2 t) - aL_2 \tag{2.13}$$

$$v'_{coss}(t) = A_1 \omega_2 \cos(\omega_2 t) - A_2 \omega_2 \sin(\omega_2 t) \tag{2.14}$$

$$i_{coss}(t) = C_{oss} \cdot v'_{coss}(t) \tag{2.15}$$

With A_1, A_2 are the constant parameters which depend on the initial conditions, ω_2 is the resonance frequency:

$$\omega_2 = 1/\sqrt{L_2 C_{oss}} \tag{2.16}$$

At the beginning of T32's turn-off, it is conducting, the initial conditions are:

$$v_{coss}(0) = 0 \rightarrow A_2 - aL_2 = 0 \tag{2.17}$$

$$i_{coss}(0) = C_{oss} \cdot v'_c(0) = 0 \rightarrow C_{oss} \cdot A_1 \omega_2 = 0 \tag{2.18}$$

$$\begin{cases} A_1 = 0 \\ A_2 = aL_2 \end{cases} \tag{2.19}$$

Replace A_1, A_2 to (2.13), (2.15)

$$v_{coss}(t) = aL_2[\cos(\omega_2 t) - 1] \tag{2.20}$$

$$i_{coss}(t) = -aL_2 \omega_2 C_{oss} \cdot \sin(\omega_2 t) = \frac{-a}{\omega_2} \cdot \sin(\omega_2 t) \tag{2.21}$$

If $t = t_{tr}$ is the moment at the end of the transient time. In the steady state, when the current slope is zero, the voltage and current of the output capacitor are similar to (2.13), (2.14), (2.15) with $a = 0$.

$$v_{coss}(t') = A_1 \sin(\omega_2 t') + A_2 \cos(\omega_2 t') \tag{2.22}$$

$$v'_{coss}(t') = A_1 \omega_2 \cos(\omega_2 t') - A_2 \omega_2 \sin(\omega_2 t') \tag{2.23}$$

$$i_{coss}(t') = C_{oss} \cdot v'_{coss}(t') \tag{2.24}$$

With $t' = t - t_{tr}$, the initial conditions of the steady state oscillation are the capacitor voltage and current in (2.20), (2.21) at $t = t_{tr}$:

$$\begin{aligned} v_{coss}(t' = 0) &= aL_2 \cos(\omega_2 t_{tr}) - aL_2 \rightarrow A_2 \\ &= aL_2 \cdot [\cos(\omega_2 t_{tr}) - 1] \end{aligned} \tag{2.25}$$

$$i_{coss}(t' = 0) = C_{oss} v'_c(t' = 0) = -\frac{a}{\omega_2} \cdot \sin(\omega_2 t_{tr}) = A_1 \omega_2 \cdot C_{oss} \tag{2.26}$$

$$\begin{cases} A_1 = -aL_2 \cdot \sin(\omega_2 t_{tr}) \\ A_2 = aL_2 \cdot (\cos(\omega_2 t_{tr}) - 1) \end{cases} \tag{2.27}$$

Replace A_1, A_2 to (2.22), (2.24):

$$v_{coss}(t') = aL_2 \cdot [\cos(\omega_2 t' + \omega_2 t_{tr}) - cos(\omega_2 t')] \tag{2.28}$$

$$i_{coss}(t') = \frac{a}{\omega_2} \cdot [\sin(\omega_2 t') - \sin(\omega_2 t' + \omega_2 t_{tr})] \tag{2.29}$$

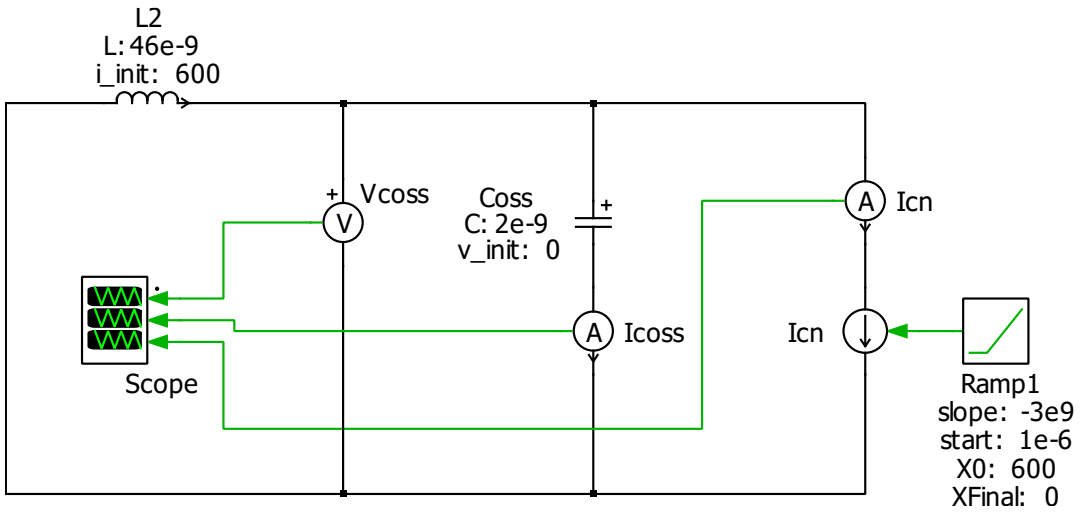


Figure 2.4: *PLECS simulation model of the HF loop triggered by current slope at input.*

To verify the analytical model in (2.20), (2.21) and (2.28), (2.29), a PLECS simulation is created like Figure 2.4. The simulation results are compared with the analytical model which are shown in Figure 2.5.

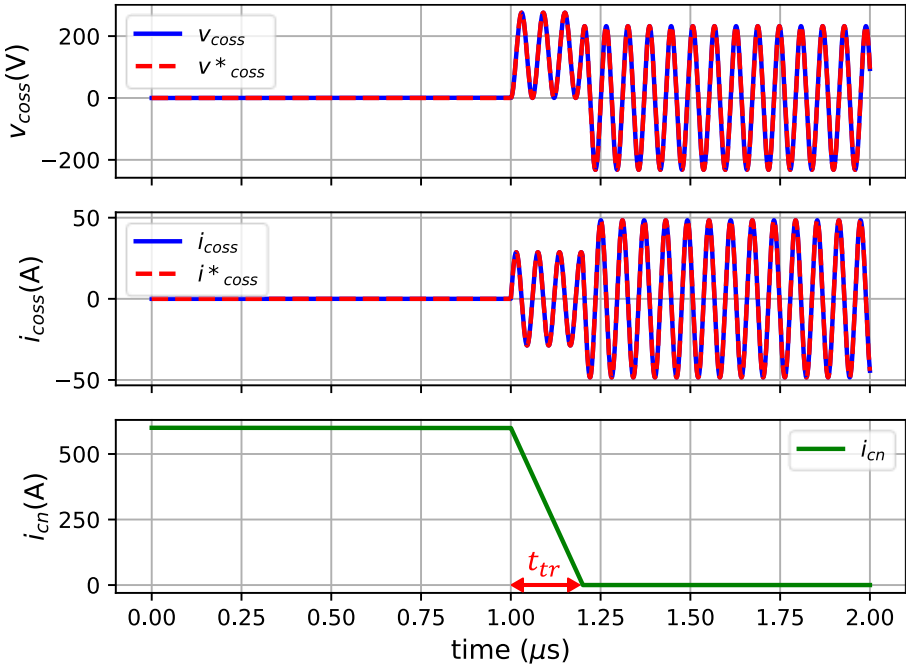


Figure 2.5: *Compare voltage and current waveforms in PLECS simulation (blue solid lines) and analytical model (red dashed line).* $t_{tr} = 200\ ns, a = -3\ A/ns$

From (2.25), (2.26), the steady state oscillation amplitudes directly proportional to the current slope a. The faster the MOSFET is switched, the larger the HF oscillation amplitude is. The HF resonance current amplitude directly depends on the ratio between the current slope a and the HF resonance frequency ω_2. From (2.28), (2.29), the initial energy of the steady state oscillation can be calculated:

$$E_0(t' = 0) = \frac{1}{2} C_{oss} v_{coss}^2(t' = 0) + \frac{1}{2} L i_{coss}^2(t' = 0) \tag{2.30}$$

$$E_0 = \frac{1}{2} C_{oss} a^2 L_2^2 \cdot [\cos(\omega_2 t_{tr}) - 1]^2 + \frac{1}{2} L \frac{a^2}{\omega_2^2} \cdot \sin^2(\omega_2 t_{tr}) \tag{2.31}$$

$$E_0 = C_{oss} a^2 L_2^2 \cdot [1 - \cos(\omega_2 t_{tr})] \tag{2.32}$$

From (2.32), it is possible to choose t_{tr} so that there is no steady state oscillation:

$$E_0 = 0 \rightarrow t_{tr} = \frac{n\pi}{\omega_2} = n\pi\sqrt{L_2 C_{oss}} \qquad (2.33)$$

From the PLECS simulation above, if n = 4, $t_{tr} = 120.4\,ns$ or $a = -4.98\,A/ns$; the steady state oscillation is canceled. The simulation and analytical results are shown in Figure 2.6. The result is used demonstrate the precise of the analytical model aligned with the simulation model even in this particular case. In real switching event, it is difficult to achieve this oscillation cancelation because t_{tr} should be very precise calculated. In fact, t_{tr} is very small and varied with the output capacitor C_{oss}, which is changed during v_{ds} transient.

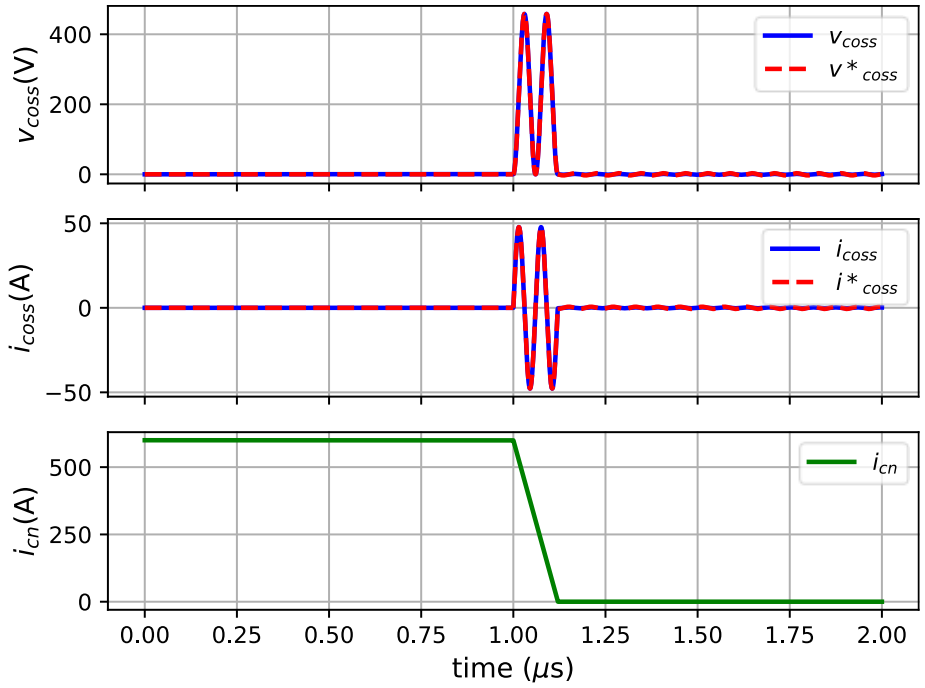


Figure 2.6: *The steady state oscillation is canceled with proper selection of current slope. n = 4,* $t_{tr} = 120.4\,ns$, $a = -4.98\,A/ns$.

According to the AC superposition theorem, in a coupled LRC circuit, v_{coss} is superimposed with $v_{cf}(\omega_1 t)$. The if consider the attenuation factor, i_{coss}, v_{coss} can be modeled:

$$i_{coss}(t) = i_{coss}(\omega_2 t) \cdot e^{-tR_2/2L_2} \quad (2.34)$$

$$v_{coss}(t) = \left[I_L \cdot \sqrt{\frac{L_1}{C_f}} \cdot \sin(\omega_1 t) + (V_{cf0} - V_{DC}/2) \cdot \cos(\omega_1 t) \right] \cdot e^{-tR_1/2L_1} + v_{coss}(\omega_2 t) \cdot e^{-\frac{tR_2}{2L_2}} + V_{DC}/2 \quad (2.35)$$

The analytical model in (2.35), (2.34) are compared with a real MOSFET's turn-off in a two-stage decoupling ANPC: V_{DC} = 1500V, IL = 560A, $t_{tr} = 125$ ns, $a = -5$ A/ns, L_1 =115nH, L_2 = 46nH, C_f = 1.6µF, C_{oss} =1.89nF, R1 = 0.095Ω, R2 = 0.24Ω. There is a correction for the voltage dropped on the stray inductance at the MOSFET's drain terminal L_d = 10nH. The results are presented in Figure 2.7.

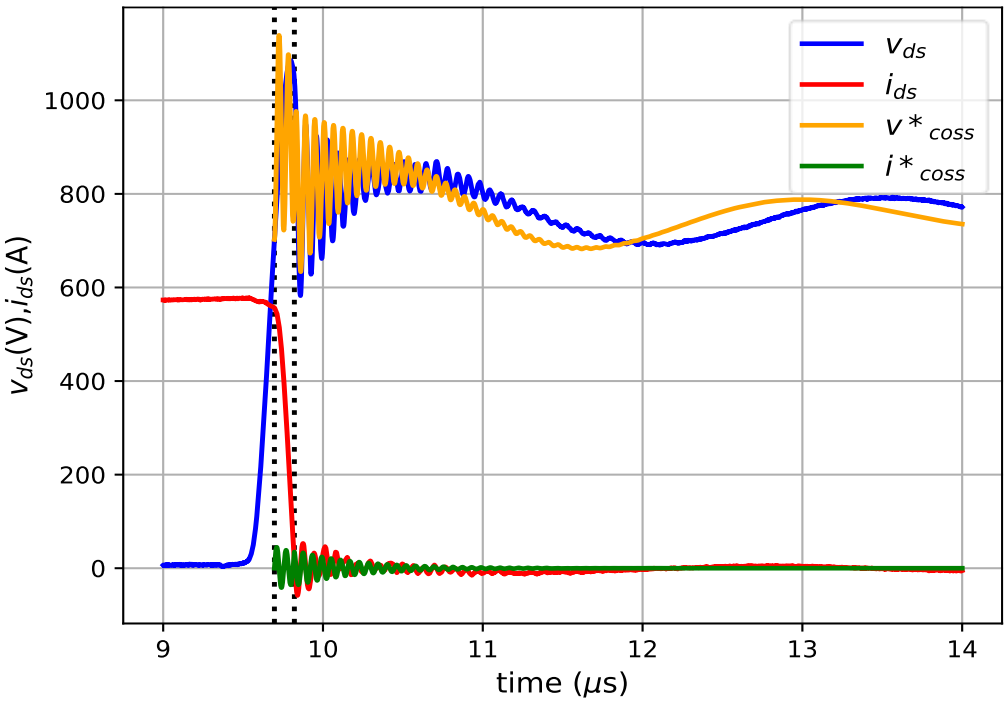


Figure 2.7: *Compare experimental turn-off voltage and current waveforms of a SiC MOSFET in the two-stage decouple ANPC (blue and red lines) with the proposed analytical model (orange and green lines).*

There are some mismatches between the analytical model and the real measurement waveform, especially during the transient due to some simplifications:

- C_{oss} is assumed to be constant. Actually, C_{oss} is changed with v_{ds}. It reduces quickly when v_{ds} approaches to nominal voltage
- The extracted parameters have their tolerances.
- The other MOSFET's voltage is considered as zero.
- Current slope is assumed to be constant.

The model provides some important understanding of the switching oscillation:

- The initial oscillation energy is proportional to $a^2 L_2^2$. Switching at high speed and large stray inductance can lead to profound oscillation and overvoltage.
- The steady state oscillation is the result of the voltage and current of the output capacitor at the end of the current transient.
- The voltage oscillation of the MOSFET is the superposition of decoupling capacitor's and output capacitor's voltages.

2.2 The unbalanced DC link oscillation in 2SiC hybrid ANPC

In the ANPC topology, a neutral point divides the DC link voltage into two distinct DC voltage sources, namely V_{DC1} on the upper side of ANPC and V_{DC2} on the lower side (as shown in Figure 2.8). It is possible that V_{DC1} may not be equal to V_{DC2} due to variations in load conditions or component tolerances. This situation is referred to as an unbalanced DC link state within the ANPC. This effect typically occurs during zero-crossing points, when the output voltage of the inverter changes its polarity.

If it is assumed that at the beginning, the switching state is on the upper side of the ANPC, T11, T21 are on, the decoupling capacitor C_f is charged to voltage V_{DC1} like in Figure 2.8a. During switching, there is a moment when the ANPC has to switch to lower side DC link (Figure 2.8b). At this moment, voltage slope at the output of the impedance network triggers only the low frequency oscillation with the initial voltage of the decoupling capacitor is $V_{cf0} = V_{DC1}$, the LF oscillation that can be seen on C_f is:

$$i_{cf}(t) = -\frac{V_{DC1} - V_{DC2}}{\sqrt{\frac{L_1}{C_f}}} \cdot \sin(\omega_1 t) \quad (2.36)$$

$$v_{cf}(t) = (V_{DC1} - V_{DC2}) \cdot \cos(\omega_1 t) + V_{DC2} \quad (2.37)$$

$$E_0 = \frac{1}{2} C_f \cdot (V_{DC1} - V_{DC2})^2 \quad (2.38)$$

$$\omega_1 = 1/\sqrt{L_1 C_f} \quad (2.39)$$

With E_0 is the initial oscillation energy of the LF oscillator. From the appendix A.1.5, since the output impedance spectrum of the coupled oscillators sees only one valley at the low resonance frequency, so there is only the low frequency oscillation is triggered. The effect may cause overvoltage on SiC MOSFET and also switching losses on the IGBT. It is important that in the design stage of the 2SiC hybrid ANPC, the designer should this effect into consideration. The unbalanced voltage should be quantified as one of the design parameters.

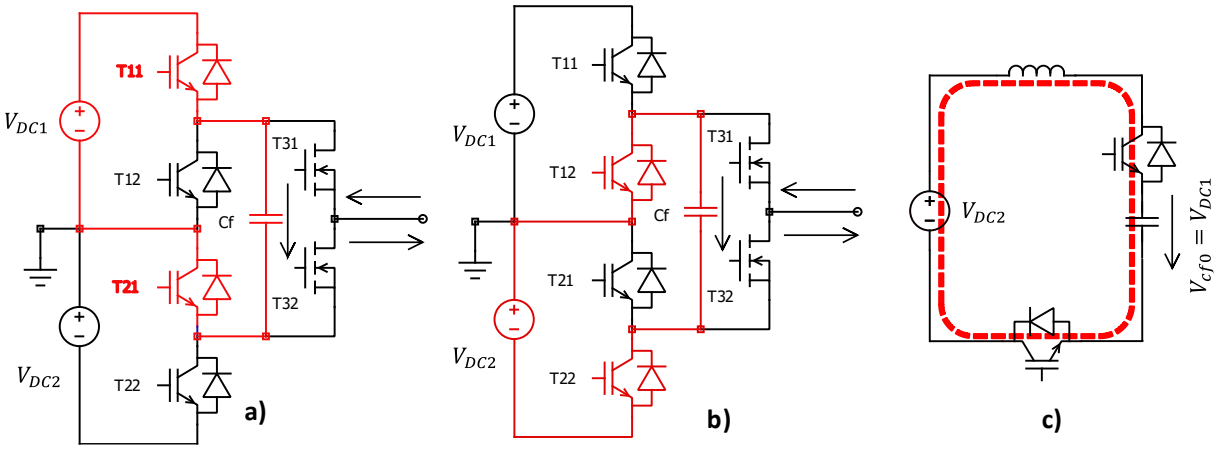


Figure 2.8: *The unbalanced DC link oscillation in 2SiC hybrid ANPC, a) C_f is charged to V_{DC1}, b) ANPC is switched to lower side DC link, c) The equivalent circuit when the ANPC is switched to V_{DC2} with the initial capacitor voltage V_{DC1}.*

To demonstrate the behavior of the decoupling capacitor during unbalanced DC link voltage, a simulation model in SIMetrix was created (Figure 2.9). It was run in 2 cases: DC link voltage is balanced at 750V and unbalanced at 900V and 600V. The load current was set at 100A. The simulation results are presented in Figure 2.11, Figure 2.12.

Figure 2.10 shows the switching timing of the simulation. The zero-crossing switching happens at t_1 = 0.5s and t_2 = 1s. The details behaviors of the circuit are explained in Table 2.1

and Table 2.2. The zero-crossing switching sequence at t_1: T11 is off → T21 is off → T12 is on → T22 is on. The zero-crossing switching sequence at t_2: T22 is off → T12 is off → T21 is on → T11 is on.

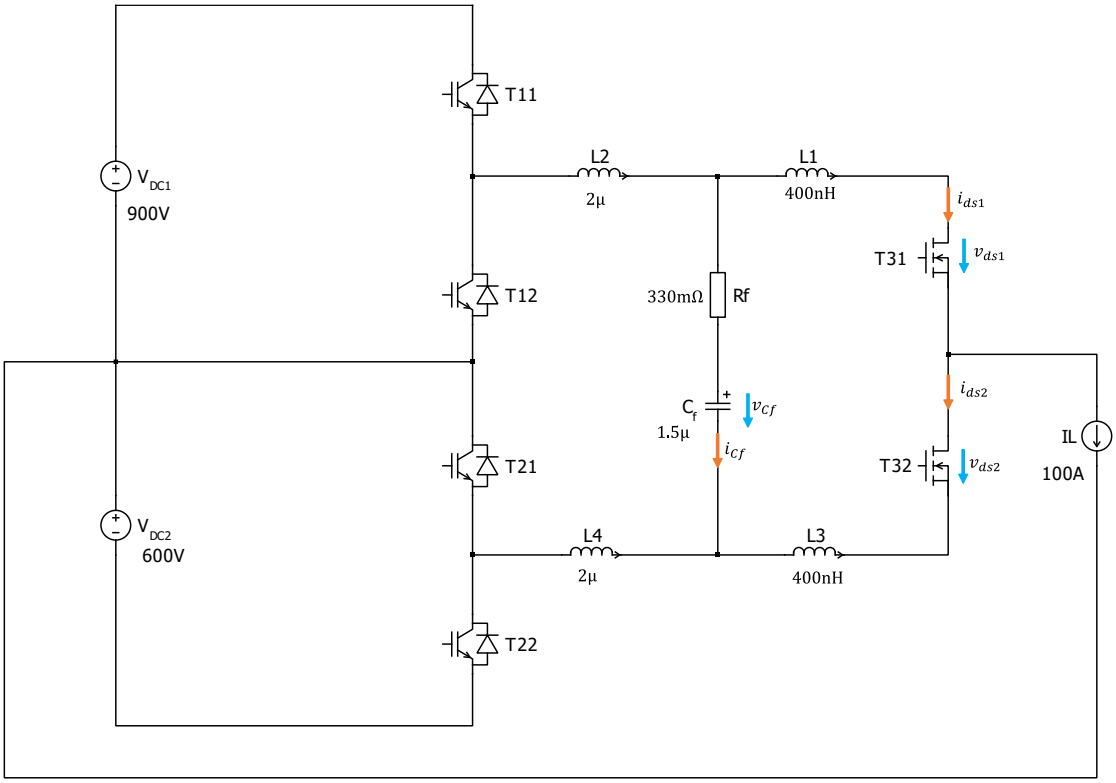


Figure 2.9: *SIMetrix simulation of the unbalanced DClink oscillation in 2SiC hybrid ANPC.*

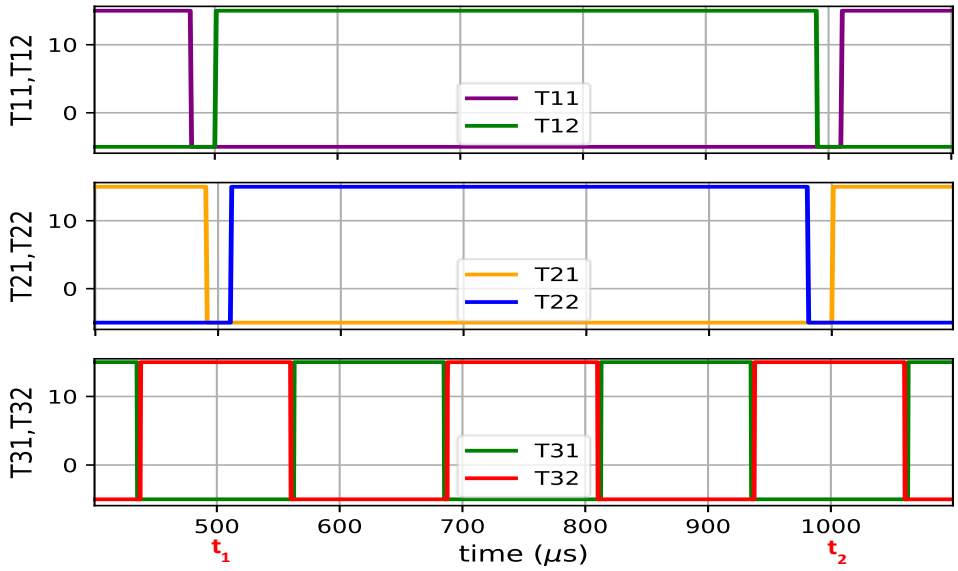


Figure 2.10: *Gate control signals of the SIMetrix simulation. t_1, t_2 are zero-crossing transitions.*

Figure 2.11 depicts how the oscillation affects the switching of SiC MOSFET. The low and high frequency loops are excited at each SiC MOSFET switching event. During zero-crossing events, there is only low frequency loop is excited by unbalanced DC link voltage. There is no oscillation if the DC link voltage is balanced. Figure 2.12 shows the voltage and current waveform of the decoupling capacitor during IGBT and MOSFET switching. Figure 2.13 shows the switching loss on IGBT T11 during the switching transition from the lower side 600V back to the upper side 900V. After T21 is closed, the voltage across T11 is 900V-600V (the initial capacitor voltage at this moment is 600V). The current goes through T11 is the LF oscillation current which is triggered by the unbalanced transition and cause the switching loss on T11.

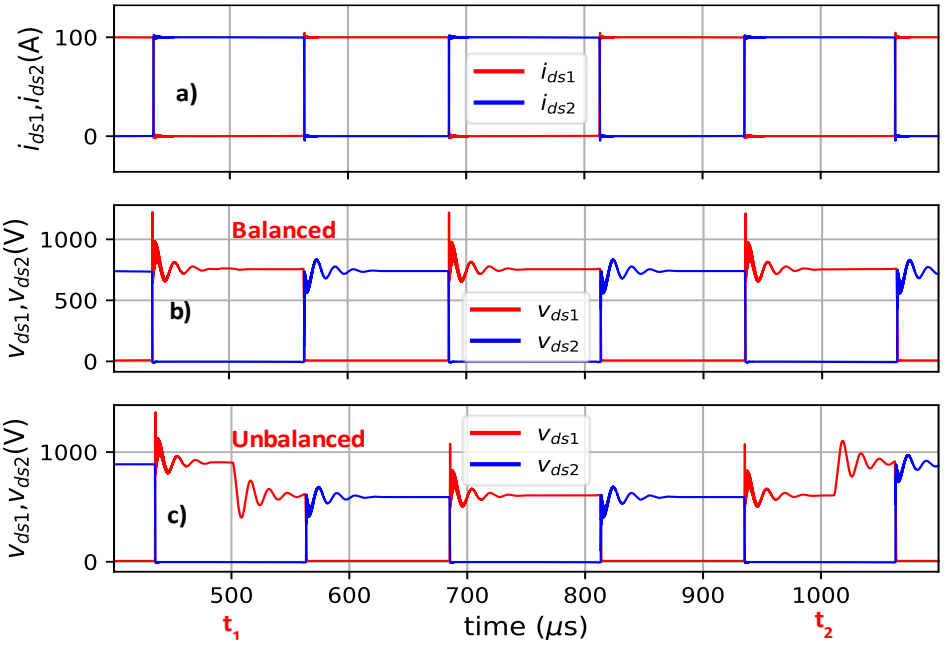


Figure 2.11: *SiC MOSFET's voltages and currents when there is balanced and unbalanced DC link voltage.*

From equation (2.36), the LF resonance current is small if L_1 is large and a small C_f is used. Since the zero-crossing happens at the fundamental frequency, the switching losses due to unbalanced DC link voltage are relatively low. However, the primary consequences are overvoltage on the SiC MOSFETs and overcurrent on the IGBTs. The most critical scenario occurs when either T31 or T32 is switched immediately after the zero-crossing, while the LF oscillation has not yet fully damped. At this moment, the new LF oscillation is triggered with

the residual energy from the previous zero-crossing oscillation. The voltage and current of the decoupling capacitor at this moment can be modeled:

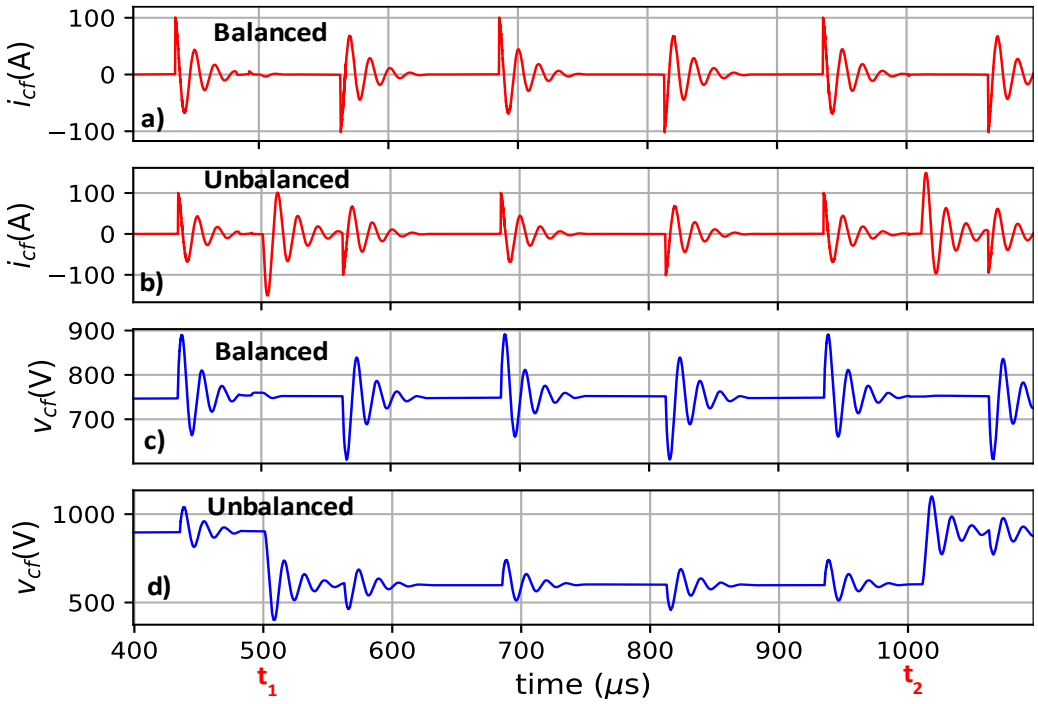


Figure 2.12: *Decoupling capacitor's voltage and current when there is balanced and unbalanced DC link voltage.*

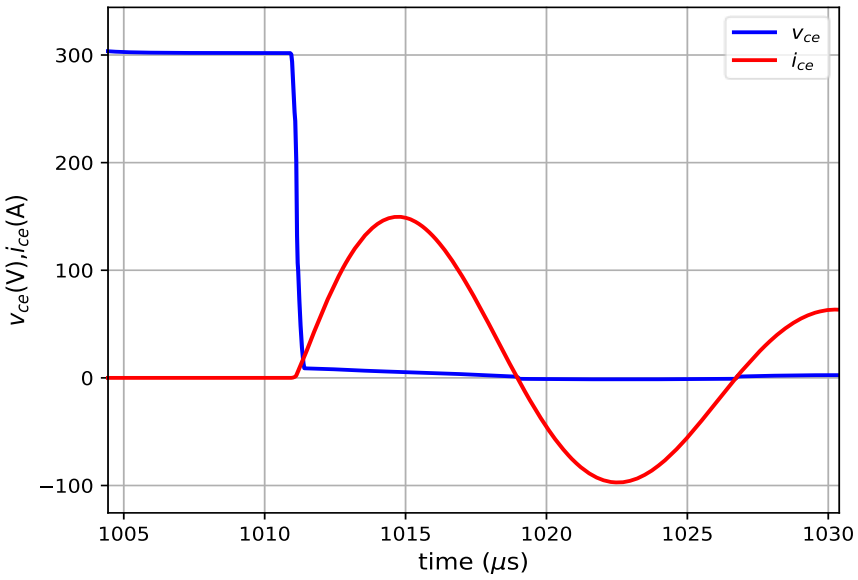


Figure 2.13: *Voltage and current across T11 during the zero-crossing transition under unbalanced DC link voltage. (Simulation result)*

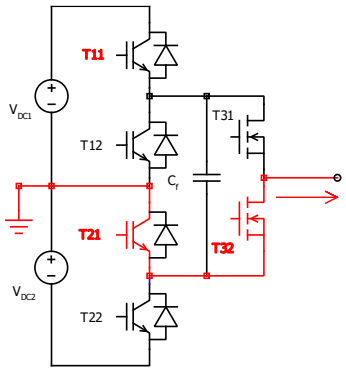
$$i_{cf}(t-t_0) = \left(I_L + i_{cf}\big|_{t=t_0}\right)\cdot\cos\left(\omega_1(t-t_0)\right) - \frac{V_{cf}\big|_{t=t_0} - V_{DC2}}{\sqrt{\frac{L_1}{C_f}}} \cdot \sin\left(\omega_1(t-t_0)\right) + i_{coss}(t-t_0) \tag{2.40}$$

$$v_{cf}(t-t_0) = \left(I_L + i_{cf}\big|_{t=t_0}\right)\cdot\sqrt{\frac{L_1}{C_f}}\cdot\sin\left(\omega_1(t-t_0)\right) + \left(V_{cf}\big|_{t=t_0} - V_{DC2}\right)\cdot\cos\left(\omega_1(t-t_0)\right) + V_{DC2} \tag{2.41}$$

With t_0 is the moment when SiC MOSFET is switched right after the unbalanced transition (for instance, from V_{DC1} to V_{DC2}). $V_{cf}\big|_{t=t_0}, i_{cf}\big|_{t=t_0}$ is the decoupling capacitor's voltage and current at t_0.

When oscillation energy accumulates after each switching, it can pose a danger overvoltage, overcurrent situation. It is crucial to cut off the oscillation before initiating a new switching, particularly the low-frequency (LF) oscillation. The switching scheme presented in chapter 4 will ensure the LF oscillation energy is fully dissipated before the new transition starts.

Table 2.1: *Switching transition at t_1 = 0.5s, IL > 0, $V_{DC1} > V_{DC2}$.*

Schematic	Note
	- The red switches are the on state switches: T11, T21, T32. - $V_{cf} = V_{DC1} > V_{DC2}$. - Load current is positive and goes out of the inverter. - All the switching oscillations are died out at this time.

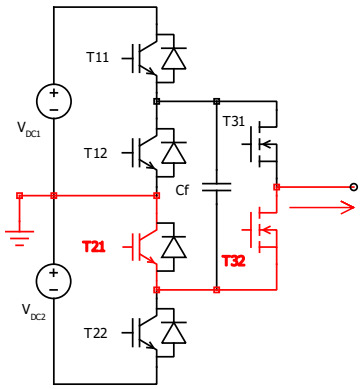
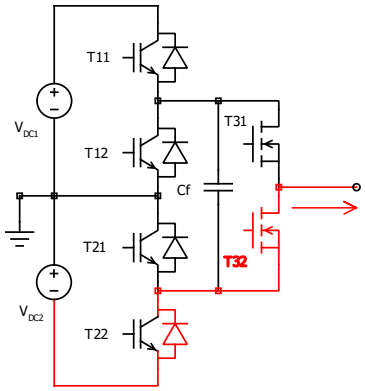
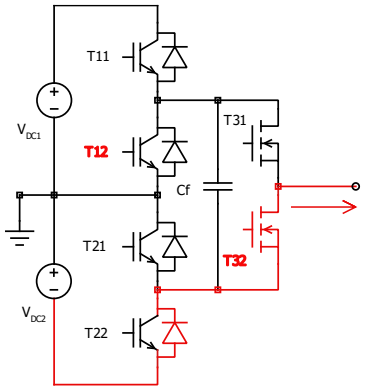
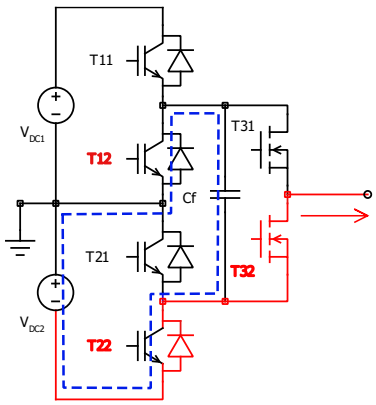
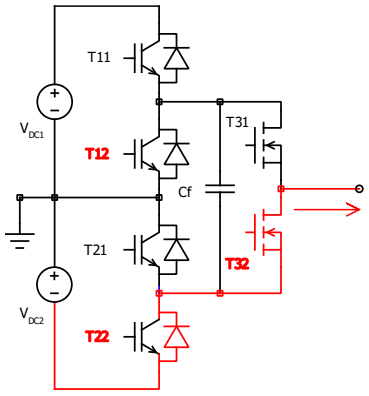
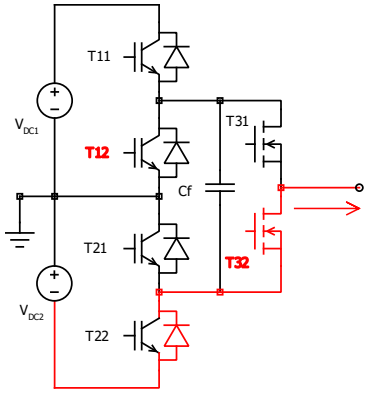
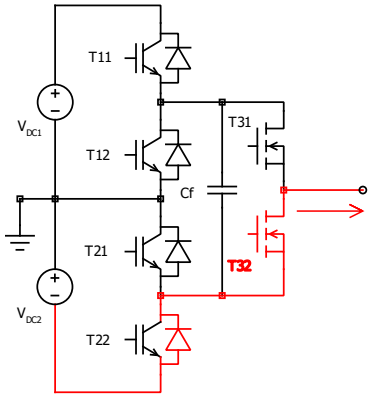
	- The outer IGBT, T11 is turned off first. - $V_{cf} = V_{DC1}$. - There is no switching loss on T11 when it is turned off because there is no current going through it.
	- When T21 is off, the load current commutates to diode D22. - $V_{cf} = V_{DC1}$. - Switching losses on T21, D22.
	- The inner IGBT T12 turn on first. - $V_{cf} = V_{DC1}$. - There are no switching losses on T12 because of no load current.
	- The outer IGBT T22 is turned on after T12. The oscillation circuit is fully closed. - The low frequency oscillation (blue dashed line) is triggered with initial current is IL and initial voltage on the decoupling capacitor is V_{DC1}. - $V_{cf} = V_{DC2}$. - There is no loss on T22 caused by the oscillation and load current because D22 is conducting.

Table 2.2: *Switching transition at t_2 = 1s, IL > 0, $V_{DC1} > V_{DC2}$.*

Schematic	Note
	- $V_{cf} = V_{DC2} < V_{DC1}$. - Load current is positive and goes out of the inverter. - All the switching oscillation is died out at this time.
	- The outer IGBT T22 is turned off first. - $V_{cf} = V_{DC2}$. - No turn-off loss on T22 because D22 is conducting.
	- T12 is turned off at no loss because no load current going through it. - $V_{cf} = V_{DC2}$.

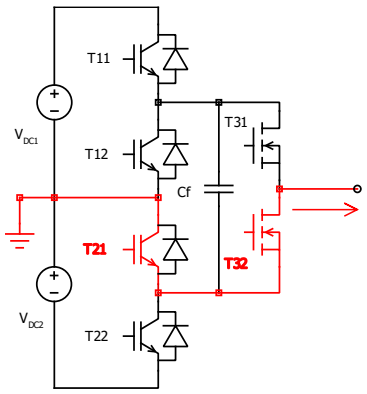
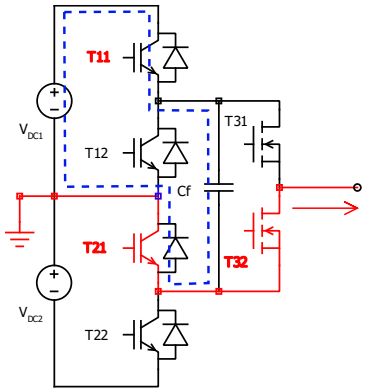
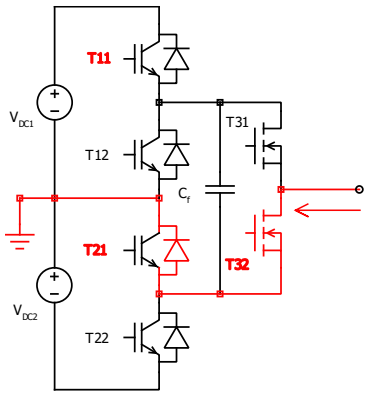
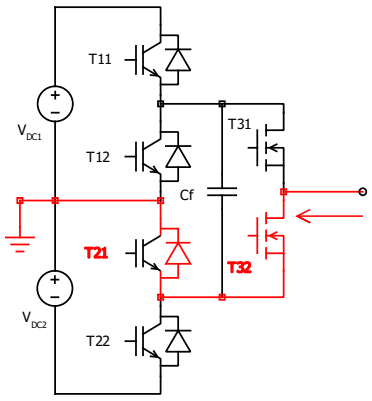
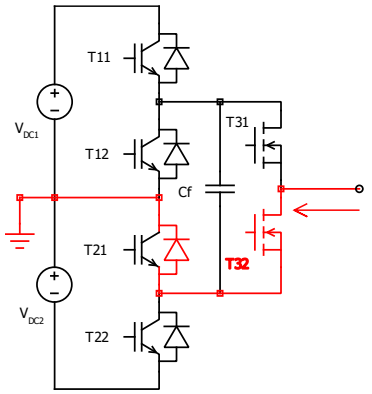
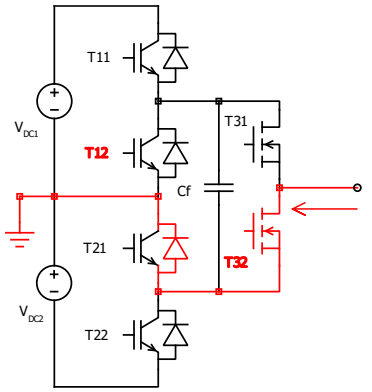
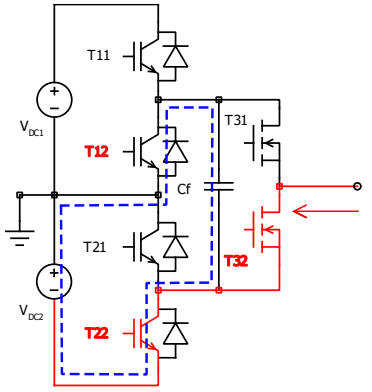
	- The inner IGBT T21 is turned on first. - There is turn-on loss on T21 because the load current goes through it. - There is reverse-recovery loss on D22. - $V_{cf} = V_{DC2}$.
	- T11 is on, the oscillation circuit is fully closed. - The low frequency oscillation (blue dashed line) is triggered with initial current IL and initial voltage on the decoupling capacitor is V_{DC2}. - Before T11 is turned on, the voltage across it is V_{DC1}-V_{DC2}, because of the voltage on the decoupling capacitor is V_{DC2}. - The oscillation starts and creates loss on T11 because of the voltage transition and the oscillation current. The transition can be seen in Figure 2.13.

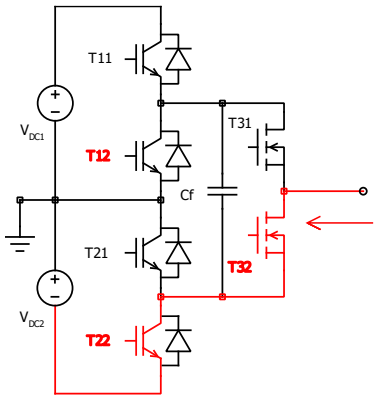
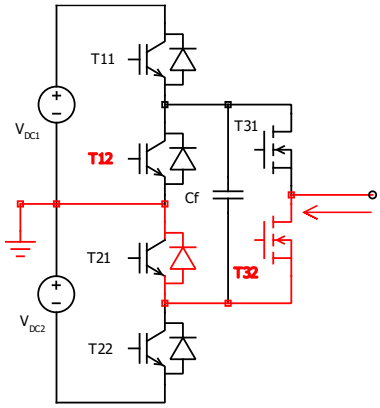
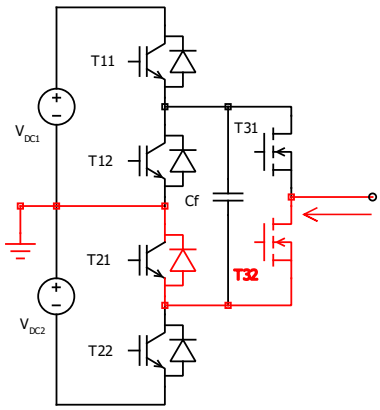
Table 2.3: *Switching transition at t_1 = 0.5s, IL < 0, $V_{DC1} > V_{DC2}$.*

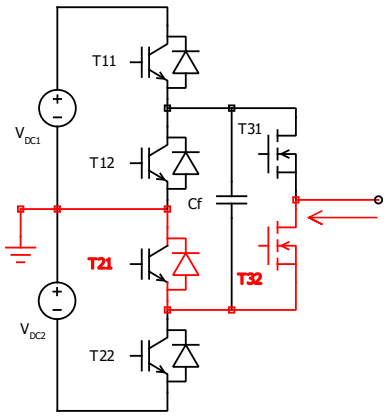
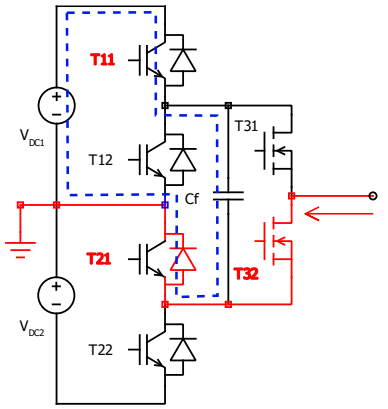
Schematic	Note
	- $V_{cf} = V_{DC1} > V_{DC2}$. - Load current is negative and goes into the inverter. - All the switching oscillation is died out at this time.

	- The outer IGBT T11 is turned off first. - $V_{cf} = V_{DC1}$. - No turn-off loss on T11 because there is no load current going through it.
	- T21 is turned off at no loss because D21 is conducting. - $V_{cf} = V_{DC1}$.
	- The inner IGBT T12 is turned on first. - There is turn-on loss on T12 because there is no load current going through it. - $V_{cf} = V_{DC1}$.
	- T22 is on, the oscillation circuit is fully closed - The low frequency oscillation (blue dashed line) is triggered with initial current IL and initial voltage on the decoupling capacitor is V_{DC1} - Before T22 is turned on, the voltage across it is V_{DC1}-V_{DC2} because of the voltage on the decoupling capacitor is V_{DC1}.

	- The oscillation starts and creates loss on T22 because of the voltage transition and the load current + oscillation current.

Table 2.4: *Switching transition at t_2 = 1s, IL < 0, $V_{DC1} > V_{DC2}$.*

Schematic	Note
	- $V_{cf} = V_{DC2} < V_{DC1}$. - Load current is negative and goes into the inverter. - All the switching oscillation is died out at this time.
	- The outer IGBT T22 is turned off first. - $V_{cf} = V_{DC2}$. - turn-off loss on T22.
	- T12 is turned off at no loss because no load current going through it. - $V_{cf} = V_{DC2}$.

	- The inner IGBT T21 is turned on first. - There is no turn-on loss on T21 because D21 is conducting. - $V_{cf} = V_{DC2}$.
	- T11 is on, the oscillation circuit is fully closed. - The low frequency oscillation (blue dashed line) is triggered with initial current IL and initial voltage on the decoupling capacitor is V_{DC2}. - Before T11 is turned on, the voltage across it is V_{DC1}-V_{DC2}, because of the voltage on the decoupling capacitor is V_{DC2}. - The oscillation starts and creates loss on T11 because of the voltage transition and the oscillation current.

In summary, the presence of decoupling capacitor establishes a coupled LCR circuit with two distinct low and high resonance frequencies. Low frequency resonance current can circulate in the LF circuit thanks to the on state IGBTs and the free-wheeling diodes. Both low and high frequencies resonances are triggered by the current slope at the input of the coupled LCR circuit. The high frequency oscillation's energy is proportional to the square of the current slope and the HF circuit's stray inductance. The steady state HF oscillation depends on the output capacitor's voltage and current at the end of the current transient.

When there is a zero-crossing under unbalanced DC link voltage, the voltage slope at the output of the coupled LCR circuit will trigger only the low frequency resonance. The LF oscillation energy is proportional to square of the voltage difference between the upper and lower DC link. The unbalance can cause switching losses, overcurrent on the IGBTs and overvoltage on SiC MOSFET.

3. High Frequency Oscillation Damping

SiC MOSFET can switch fast with low switching losses, but the fast switching comes along with the undesirable high oscillation or ringing [33-34]. Those undesirable oscillations can add the overvoltage and switching losses to the devices and introduce more the electromagnetic interference (EMI), which reduces the reliability of the whole system [35, 36]. The switching oscillation of SiC MOSFET is in MHz range which stays in the definition of EMI conduction frequency range of FCC 15 regulation and CISPR22 and EN55022 standard [35]. Damping the switching oscillation is crucial for the system reliability especially in high power applications. There are many damping methods were investigated in literature and these methods can be categorized into three primary groups, each with distinct damping mechanisms.

1. Energy reduction: The first group focuses on reducing the oscillation energy stored within the circuit. This is achieved by diminishing stray inductance in the circuit through the optimization of busbar, PCB, or module layout designs [39-43]. While optimizing stray inductance is a standard practice in inverter design, it's not always feasible, particularly in high-power 2SiC hybrid ANPC applications.

2. Excitation source reduction: The second group aims to reduce the excitation source by slowing down the switching speed, often by employing high gate resistors [38, 47-49]. However, this method effectively reduces oscillations but comes at the cost of increased undesired switching losses. Furthermore, suggestions involving active gate drivers (AGD) [55-57] partially reduce switching speed during specific transient periods. Nevertheless, these solutions require sophisticated gate driver designs and tuning schemes, which can be considered a drawback.

3. Energy Dissipation: The third group concentrates on dissipating oscillation energy faster as losses on a loop's resistor [38, 44, 45, 46]. A common technique within this group is the use of an RC snubber, which offers high damping resistance to the oscillator at high frequencies. However, it is more suitable for low-power applications with minimal stray inductance and low load currents. In scenarios involving high power, high switching speeds, and extensive stray inductance in the commutation loop, the RC snubber method is not

applicable due to the high-power resistors is limited by cooling constraints and introducing extra stray inductance into the commutation loop. An alternative approach, as reported in [38], proposes the use of low-Q ferrite cores in the power circuit to mitigate oscillations. However, it's essential to note that this paper primarily provides experimental results for low-power applications and lacks a comprehensive explanation of the underlying mechanisms governing the behavior of the ferrite core during switching transients, particularly concerning overvoltage during turn-off due to the additional inductance introduced by the ferrite core.

In 2SiC hybrid ANPC there are two oscillators in cascade: high frequency oscillator and low frequency oscillator. Because of the difference in frequency, oscillation energy and position of the oscillator, there will be different damping techniques separately for each type of oscillator.

To damp the high frequency oscillation in this high-power application, a skin-effect RC snubber and dual ferrite cores are used.

3.1 Skin-effect decoupling capacitor

When a RC snubber is put in place of the decoupling capacitor like in Figure 3.1, the total resistance of LF oscillator and HF are increased with R_{sn} value. The attenuation factors of the low frequency and high frequency loop are also increased.

$$\alpha_1 = \frac{R_1 + R_{sn}}{2L_1}, \alpha_2 = \frac{R_2 + R_{sn}}{2L_2} \quad (3.1)$$

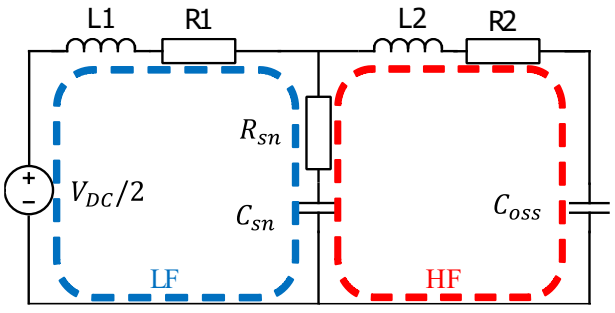


Figure 3.1: *2SiC Hybrid ANPC oscillator equivalent circuit with RC snubber.*

The advantage of employing RC snubber in this position is that it can damp both low and high frequency oscillator without DC losses on the resistor. If it is assumed that in the worst-

case scenario, all the oscillation energy in the inductor L_1 and C_f are dissipated on R_{sn}, according to the snubber design guideline in [32], the RC snubber circuit values can be estimated in equations (3.2), (3.3) with C_{sn}, R_{sn}, PR_{sn} are snubber capacitor, snubber resistor, power losses on snubber resistor values. IL_{max} is the maximum load current, V_{SOA} is the safe operating voltage (SOA), f_{sw} is the switching frequency, t_r is the turn-on current rising time.

$$C_{sn} = \frac{L_1 IL_{max}^2}{(V_{SOA} - V_{DC}/2)^2} \quad (3.2)$$

$$R_{sn} = \frac{1}{6 \cdot C_{sn} \cdot f_{sw}} \quad (3.3)$$

$$PR_{sn} = \frac{1}{2} \cdot C_{sn} \cdot f_{sw} \cdot (V_{SOA}^2 - V_{DC}^2/4) + 1.125 \cdot f_{sw} \cdot \frac{L_1^2 IL_{max}^2}{t_r \cdot R_{sn}} \quad (3.4)$$

In this 500kW 2SiC hybrid ANPC experimental setup, the stray inductance loop is large, around 115nH, $IL_{max} = 600$A, $V_{DC}/2$ = 900V, $V_{SOA} = 1200\,V$, switching frequency $f_{sw} = 10\,kHz$, t_r = 219ns. The snubber capacitor and resistor are need: $C_{sn} = 204nF, R_{sn} = 81.5\Omega, PR_{sn} = 647\,W$. It is evident that, given the combination of high load current, rapid switching speeds, and large parasitic inductance, the power loss dissipated on the snubber resistor becomes significantly high. The 650W resistor's dimensions are large which adds high stray inductance to the switching circuit. Moreover, the resistor may need active cooling to avoid overheating. Consequently, the damping approach employing a normal RC snubber is not a practical solution in this specific scenario.

To increase the loop resistance especially at the high frequency without those above disadvantages of the conventional RC snubber, the author suggests to use a special decoupling capacitor like in Figure 3.2a. The capacitor is a conduction cooled capacitor [59], which has very low parasitic inductance < 3nH and can handle high RMS current. Another advantage of this capacitor is its small size 60mm x 60mm x30 mm so it is easy to install on top of the busbar. To increase the damping capability, the skin effect is also considered when choosing the material of the steel plates.

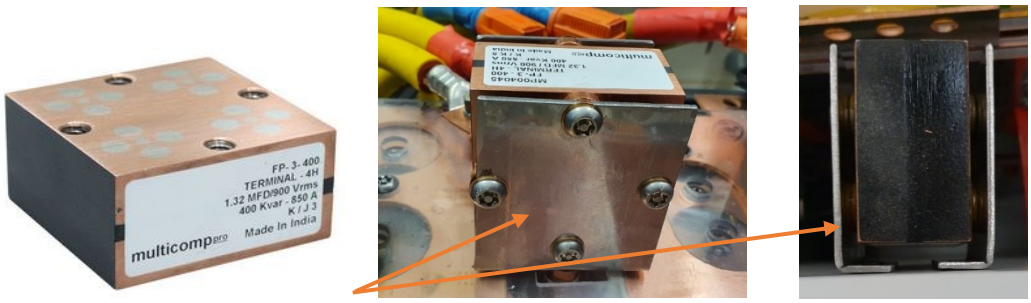


Figure 3.2: *The skin-effect decoupling capacitor a) conduction cooled capacitor b) stainless steel plates.*

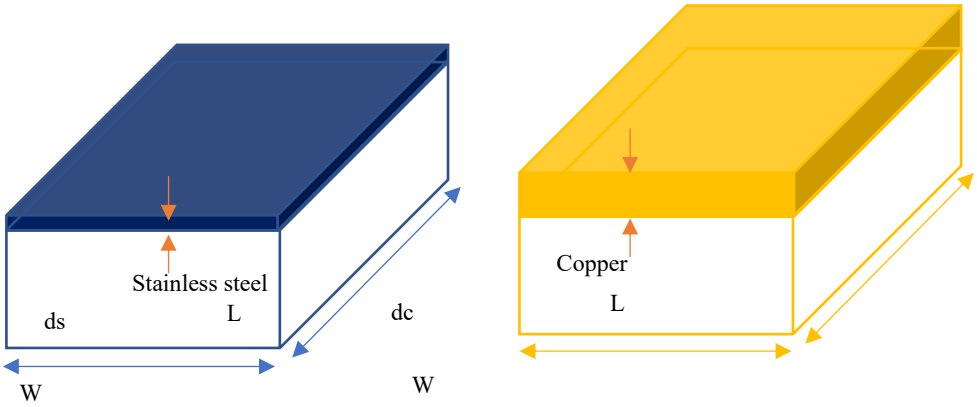


Figure 3.3: *The skin effect of different conduct material.*

It was described in [58] that the depth of the penetration of the high frequency current is governed by the skin effect. It depends on what type of material, frequency and can be calculated as:

$$d = 1/\sqrt{\pi f \mu \sigma} \tag{3.5}$$

With f is the current's frequency, μ, σ is the permeability and conductivity of the material. If there are two plates with the same size but different material: stainless-steel, index with s and copper index with c, their high frequency resistances ratio is:

$$\frac{R_c(f)}{R_s(f)} = \frac{\frac{\rho_c . L}{W \cdot d_c}}{\frac{\rho_s \cdot L}{W \cdot d_s}} = \frac{\sigma_s \cdot d_s}{\sigma_c \cdot d_c} = \frac{\sigma_s \cdot \sqrt{\pi f \mu_c \sigma_c}}{\sigma_c \cdot \sqrt{\pi f \mu_s \sigma_s}} = \sqrt{\frac{\mu_c \rho_c}{\mu_s \rho_s}} \tag{3.6}$$

To have larger high frequency resistance, the material should have $\mu_s\rho_s > \mu_c\rho_c$ with ρ_c, ρ_s are resistivity of copper and stainless steel correspondently. Table 3.1 shows the resistivity and relative permeability of some common metals. Ferritic stainless steel has the highest product $\mu \cdot \rho$ among other metals. The ferritic stainless steel X6Cr17 (EN1.4016 or AISI 430FR) has the resistivity of 0.6 μΩ.m and the relative permeability of 1800 [63] was used to make the capacitor's plates, which is expected to have 250 times more high frequency resistance than copper. The combination of stainless-steel plates and the conduction cooled capacitor make a special RC snubber circuit which can damp both LF and HF oscillator. In addition, the capacitor has low parasitic inductance and it can be fit well on top of the busbar. Another benefit of using those stainless-steel plates is that they are outside of the capacitor, which make them easily to cool down.

In order to evaluate the damping effectiveness of this unique RC snubber, a double pulse test is arranged. The turn-off voltages of the MOSFET are measured under two cases: using the conventional film capacitor and employing the skin-effect capacitor. The measurement result is shown in Figure 3.4. Both low frequency and high frequency are damped. The high frequency tends to be damped more effectively because of the skin effect. The overvoltage is smaller compare to the conventional capacitor mainly due to its low parasitic inductance.

Table 3.1: *Common metals and their resistivity, permeability.*

Metal	**Resistivity ρ (μΩ.m)**	**Relative Permeability (μ_r)**	**$\mu_r \cdot \rho$ (μΩ.m)**
Iron (99.8% pure Fe)	0.0971	5000	485.5
Electrical steel	0.082	4000	328
Ferritic stainless steel	0.58-0.62	1000-1800	580-1116
Martensitic stainless steel	0.6-0.8	750-950	450-760
Copper	0.0172	0.9999	0.0172
Aluminum	0.0265-0.0282	1	0.0265-0.0282

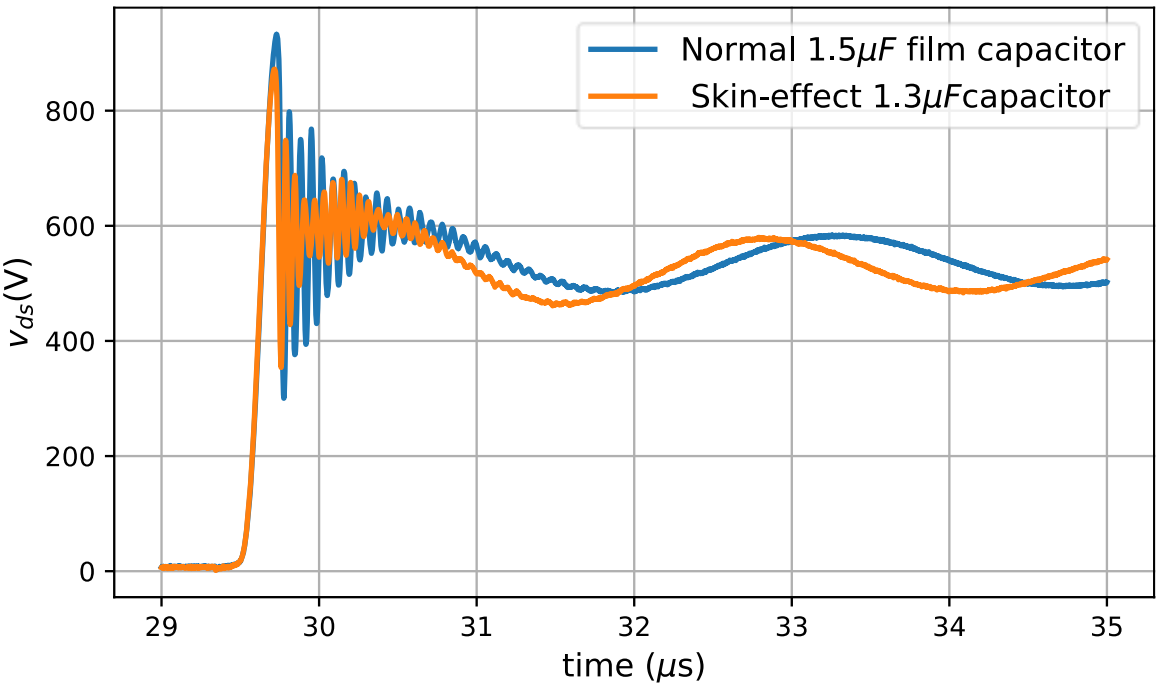


Figure 3.4: *The experimental result of the turn-off voltage across SiC MOSFET using normal 1500nF film capacitor and 1300nF special capacitor with stainless steel plates.*

3.2 Dual soft-ferrite cores

Ferrite cores are well known for effectively suppressing high frequency common mode current in the cable [60, 61]. In power electronics, the ferrite cores are inserted in the power loop to damp the switching oscillation [38, 62, 65, 93]. All the publications focus on low power applications and discrete devices. In those publications, only single core was investigated without detail information about the core's behaviors at turn-on and turn-off. In this dissertation, dual ferrite cores are first time used for damping the switching oscillations in high power application for both turn-on and turn-off. The soft ferrite materials are chosen to damp the MHz oscillation with minimum overvoltage at turn-off. The double pulse test and continuous running experimental results are presented.

3.2.1 Magnetic field inside a linear magnetic material

Figure 3.5 shows a toroidal core has the inner radial r_i, the outer radial r_o, the length is h and the effective radial r_e, $r_e = (r_i + r_o)/2$.

If there is a current I goes through it, the magnetic field strength H in the middle of the ring according to Ampere law is:

$$H = \frac{I}{2\pi r_e} \quad (3.7)$$

If the ring is the linear material (Al, Cu, air…) which has constant linear relative permeability μ_r, the flux density B which is induced by the field strength H is

$$B = \mu_r \mu_0 H \quad (3.8)$$

With $\mu_0 = 4\pi 10^{-7}$ (H/m) is the permeability of vacuum. The flux Φ inside the ring is

$$\Phi = \frac{I \mu_r \mu_0 h}{2\pi} \cdot ln\left(\frac{r_o}{r_i}\right) \quad (3.9)$$

The self-inductance of the core can be calculated:

$$\mathrm{L} = \frac{\Phi}{\mathrm{I}} = \frac{\mu_r \mu_0 h}{2\pi} \cdot ln\left(\frac{r_o}{r_i}\right) \quad (3.10)$$

If the material of the ring is linear, its permeability is a constance. Consequently, B and H have a linear relation (Figure 3.6a red dashed dot line). Its permeability can be calculated as:

$$\mu = \frac{B}{H} = constant \quad (3.11)$$

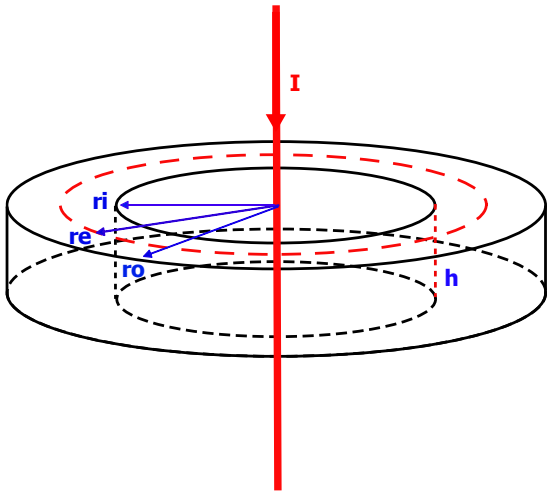


Figure 3.5: *The toroidal ferrite core is excited with current I.*

3.2.2 B-H curves of non-linear magnetic materials

If the ring is made of non-linear magnetic material (ferromagnetic, ferrite, …), the relation between B and H is no longer linear and it is presented by the B-H curves [71, 82, 97] (Figure 3.6a brown line). It should be noticed that equation (3.8), (3.9), (3.10) are only valid for isotropic material and they are not valid for anisotropic and hysteresis material like ferromagnetic and ferrite [97].

At the beginning when there is no external field applied and the ring has no magnetization. If the field strength increases from that virgin state, the flux density flows in the ring is proportional to the field strength H at the rate of μ_i which is called the initial permeability (Figure 3.6a brown dashed line). When the external field strength reaches the saturation point Hs, the flux density also reaches its maximum value Bs. If the field strength is reduced, the flux density B now doesn't follow its initial path but it follows descending branch of the hysteresis B-H curve up to the negative saturation and back to positive saturation on the ascending branch. When H is zero, the flux density doesn't go to zero but remains at the membrane flux density Br. When H reaches demagnetization force or coercivity Hc, the flux density is reset to zero.

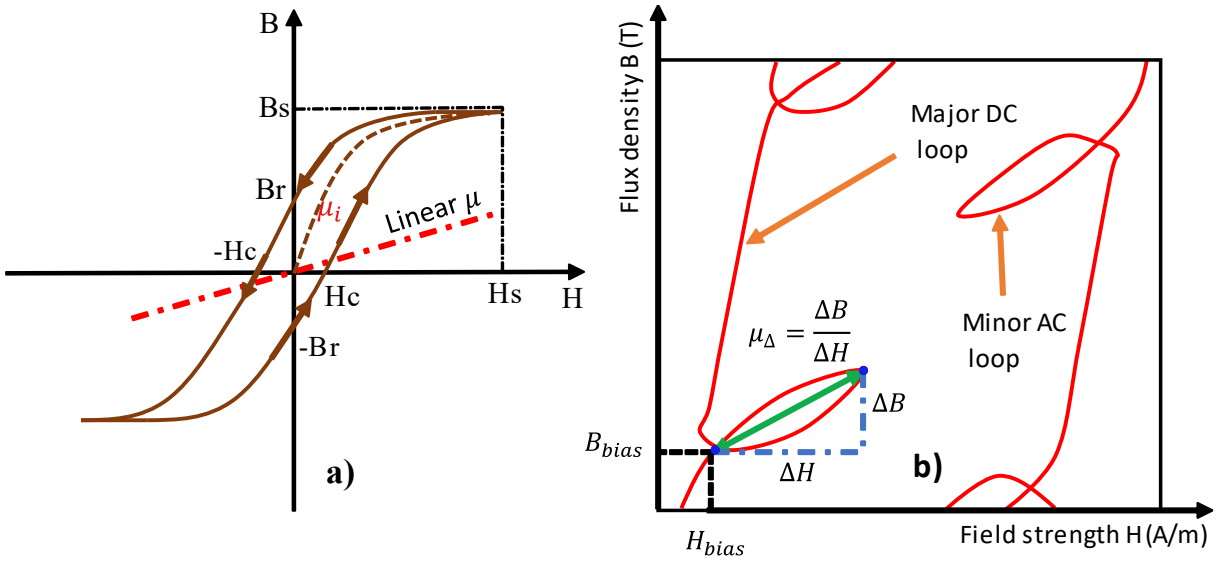


Figure 3.6: *B-H curves of none-linear magnetic material: a) Major DC loop when the material is under slow and large signal field strength, b) Major DC loop superposition with the small signal minor AC loops. The incremental permeability of the minor loop μ_Δ is the slope of the minor loop at H_{bias}, B_{bias}.*

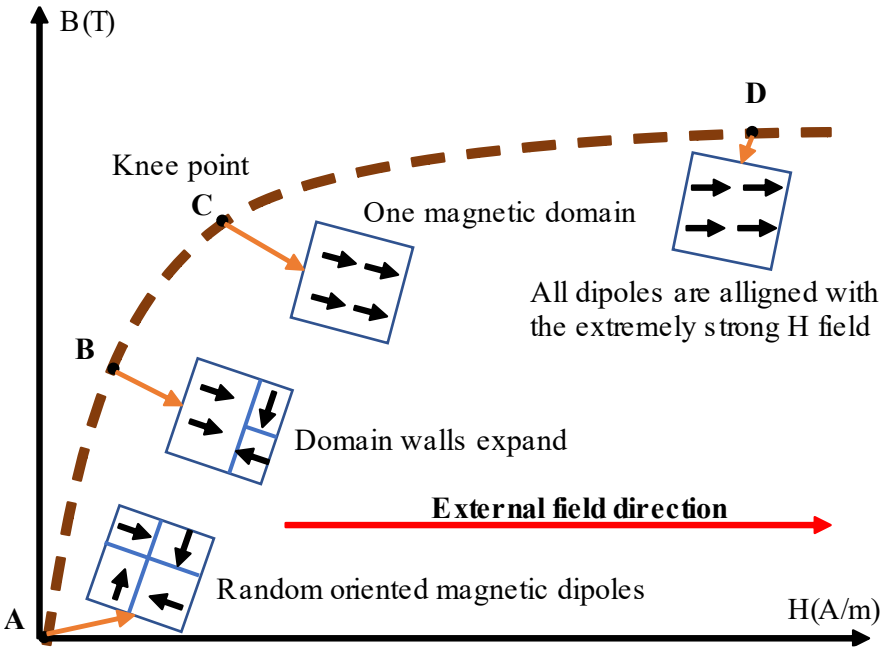


Figure 3.7: *Magnetic domains' behaviors along the one branch of the B-H curves, black arrows are the domain's magnetic dipoles, magnetic domains are presented with the rectangles.*

The nonlinear property of the magnetic material comes from its magnetic domains, that is a region of the material in which many magnetic moments are aligned in parallel [82, 83]. Those magnetic domains are different in size and have the magnetization dipoles in random directions (Figure 3.7, point A). The total magnetization of the material is zero when there is no external field. The borders between domains are called domain walls. The size of the domain depends on the balance of different internal energy [87]. When the external field is applied, the domains which nearly aligns with the external field will extend its domain walls and the others magnetic domains will be shrank (Figure 3.7), this is called domain walls' movement (Figure 3.7, point B). More and more magnetic dipoles are now oriented to the external field when the domain walls are expanded, consequently the flux density of domain increases and hence total flux density is increased. The movements of the domain walls decide the B-H curves shape. If there is an oscillating field applied on the material, the domain walls move back and forth follow the field strength. If the external field keeps increasing until when all others domains are vanished and only one domain remains (Figure 3.7, point C), the material enters its saturation region at the knee point where the permeability of the material is dramatically reduced compare to its initial permeability. After this moment, the domain walls' movement have no effect to the total flux density but the rotations of the magnetic dipoles are the main contribution because

the magnetic dipoles have not yet been aligned to the external field. The magnetic dipoles only align to the external field's direction under extremely high excitation which is rarely seen in ordinary applications, at that time, the material is completely saturated and its permeability become vacuum permeability (Figure 3.7, point D) [95].

There are some popular nonlinear magnetic materials like ferromagnetic and ferrite, amorphous alloy, nanocrystalline. Based on how large is the strength of demagnetization field Hc (coercivity), the magnetic materials are divided into soft, semi hard and hard material [72, 82].

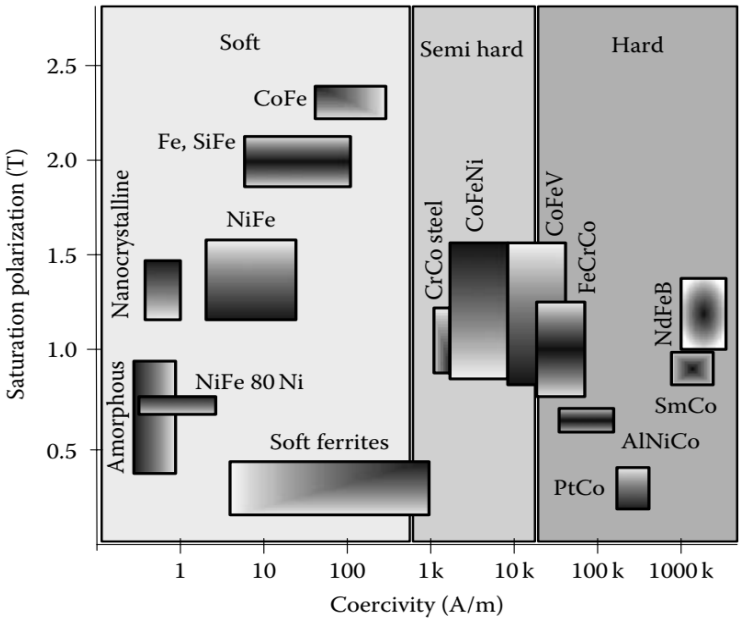


Figure 3.8: *Different type of non-linear magnetic material based on Coercivity [72].*

In this dissertation, the iron powder (ferromagnetic) and ferrite (ferrimagnetic) are investigated for high switching noise suppression. Iron powder is a soft ferromagnetic material made of iron powder and resin. The mixture is pressed under high pressure to form the core shape. Ferrites are a ceramic material which is a mixture of Fe_2O_3, and small portion of metallic elements: Mn, Zn, Ni, Mg. Ferrite materials are divided into soft ferrite and hard ferrite materials. Soft ferrite material such as MnZn or NiZn has low coercivity, hard ferrite material such as strontium and barium ferrite have higher coercivity. Soft ferrite materials usually have higher initial permeability and lower saturation field strength than iron powder. Figure 3.9 plots the first plan of BH curves from soft ferrite MnZn T35 from TDK (blue line) and ferromagnetic

iron powder (red line) FE893 from Sumida. The saturation field strength of iron powder is much higher than the soft ferrite.

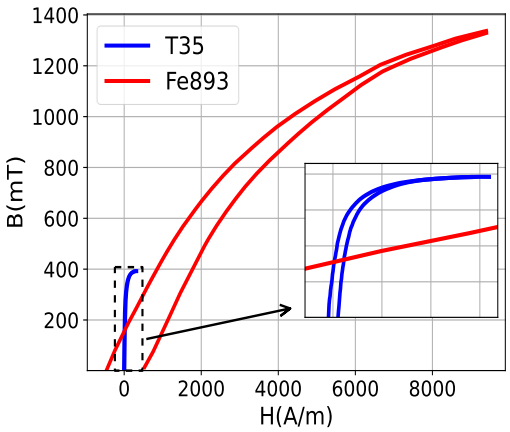


Figure 3.9: *B-H curves of soft ferrite MnZn T35 [73] and iron powder Fe893 [74].*

Table 3.2: *Compare Iron powder FE893 core and soft ferrite T35 core properties.*

	Soft ferrite	**Iron powder**
Manufacture /name of material/ serial number	TDK/T35/ B64290L0638X035	Sumida/ Fe 893/ 2353289311
Hs (A/m) @ 25C	325	30000
Size: Do/Di/h(mm)	22.1/13.7/6.35	21.5/12/10
Initial permeability μ_i (B < 0.5mT)	6000	110
Curie Temperature (°C)	130	130
Saturation current (A)	18	1578

Table 3.2 compares the properties of iron powder material Fe 893 from Sumida and the soft ferrite material MnZn T35 from TDK. The iron powder core saturates at 1578 A which is 82 times higher than MnZn (calculated corresponding to the same core's size). But the initial permeability is 54 times lower.

3.2.3 DC-bias superposition and saturable inductor

Because of the low saturation field strength, the soft ferrites are normally used with AC signal with zero DC offset. For instance, in applications like the cable ring cores for EMI suppression or the common mode chokes, where the current flows out and returns in the core simultaneously, the fluxes generated by the forward and return currents cancel each other out. Consequently, no static or DC magnetic field bias the core. When there is an unbalanced current or a DC current goes through the core in one direction, it biases the core with a DC magnetic field. If there are also high frequency, small alternating signals on top of the DC bias current, the effect is called DC-bias superposition [75-78]. Figure 3.6b shows a magnetic core is under DC biased at point A (H_{bias}, B_{bias}) and the small signal alternating field $\Delta H, \Delta B$ is applied. The small signal follows its minor loop which has the incremental permeability μ_Δ is the slope of the minor loop. The incremental permeability is the average permeability of the whole minor loop and it is constant at the bias point, which can be calculated:

$$\mu_\Delta = \frac{\Delta B}{\Delta H} \qquad (3.12)$$

The core's magnetic flux φ is changed when the excited current changes. Consequently, its self-inductance is varied with the applied current. At low current, because of the high initial permeability, the core's inductance is also high. When the exciting current goes beyond the saturation level, the core's permeability and its inductance are significantly reduced. Usually, the designer avoids to use the core out of its saturation zone. But there are some exceptions where the core is intendedly used in the saturation region [89]. For example: in [90, 91], a saturable inductor is used as an inductance turn-on snubber to reduce the turn-on losses, in [92] the reverse-recovery effect is reduced by using saturable core inductor. In [93], B. Wunsch showed that the nonlinear effect during saturation and hysteresis can help to improve the EMC filter's performance.

3.2.4 The ring ferrite core's differential inductance

Ferrite and ferromagnetic material are none-linear magnetic material, which have their permeabilities changed with the excitation field [10, 11]. Their materials' nonlinear properties are presented by the B-H loop (Figure 3.6a). When there is a current i goes through it, the voltage drops on the core will be:

$$V_{core} = \frac{d\Phi}{dt} = \underbrace{\frac{d\Phi}{di}}_{L_\Delta} \cdot \frac{di}{dt} \quad (3.13)$$

With Φ is the flux which is induced into the core by the excitation current i. The quantity $\frac{d\Phi}{di}$ can be considered as the core's differential inductance L_Δ which is a function of the excitation current. In case of a toroidal core, the flux inside the core can be calculated as:

$$\Phi = i \cdot \mu(i) \cdot \frac{h}{2\pi} ln\left(\frac{r_o}{r_i}\right) \quad (3.14)$$

With $\mu(i)$ is the core material's permeability and it is a function of the excitation current i and it equal to the slope of the B-H curves. The differential inductance of the core L_Δ can be calculated as:

$$\mathrm{L}_\Delta = \frac{d\Phi}{di} \quad (3.15)$$

$$\mathrm{L}_\Delta = \frac{h}{2\pi} ln\left(\frac{r_o}{r_i}\right) \cdot \frac{d(i \cdot \mu(i))}{di} \quad (3.16)$$

When a core carries a DC current, it becomes biased at the B_{bias} and H_{bias} points along the major B-H loop of the material (refer to Figure 3.6b). In the presence of a small AC signal current superimposed on the DC current, the trajectory of the small signal flux density B and field strength H follows a path along the minor B-H loop around the DC bias point (as illustrated in Figure 3.6b). Under this small signal excitation, the average permeability (μ_Δ) of the minor loop is considered to be constant. The differential inductance of the toroidal core at this DC bias is approximated:

$$\mathrm{L}_\Delta \approx \mu_\Delta \cdot \frac{h}{2\pi} ln\left(\frac{r_o}{r_i}\right) \quad (3.17)$$

The differential inductance of the core is changed with the DC bias current and it can be divided to three regions: weak saturation, roll-off and deep saturation region like in Figure 3.10 [99].

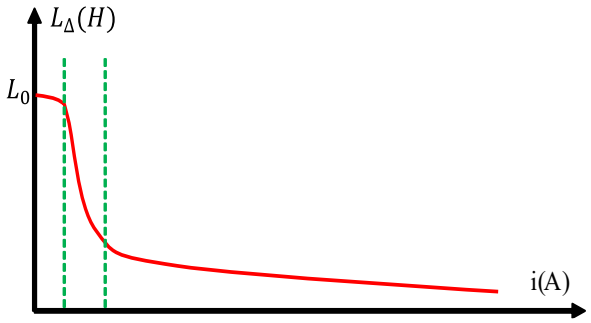


Figure 3.10: *Differential inductance of the ferrite core in different regions of the excitation current [99].*

The nominal inductance L_0 of the core is the initial inductance when the core is at very low excitation near to zero. It can be calculated:

$$\mathrm{L_0} = \frac{AL}{N^2} = AL \qquad (3.18)$$

With AL is the permeance of the core which is usually provided by the manufacture. N is the number of turns that the copper wire wraps around the core. In this application, N = 1.

3.2.5 Deep saturation core's inductance measurement

The core's material information in weak saturation and roll-off region are regularly provided by the manufacture, but there is lack of information about the material in deep saturation region. In this dissertation, author suggests a simple single pulse setup to measure the differential inductance of the ferrite core under DC bias. The information is important for the selection of the core that can damp the oscillation but doesn't add too much overvoltage at the turn-off.

The setup is very similar to the double pulse test setup with additional decoupling capacitor C_f, the core is position on the upper branch of the circuit and in front of the decoupling capacitor like Figure 3.11a. The Rogowski coil RG1, RG2 are used to measure the high frequency and bias current going through the core under test.

When T32 is on, the load current flows linearly to the lower branch. When the load current reaches the measurement point, T32 is turned off, the load current is commutated to the core at constant value, it creates a constant DC bias field inside the core. When T32 is off, the transient

current slope triggers the oscillation circuit (blue dashed line in Figure 3.11a). The core inductance at this DC bias current can be extracted from the resonance frequency f_{osc} as:

$$L_{core} = \frac{1}{4\pi^2 f_{osc}^2 C_f} - L_2 \qquad (3.19)$$

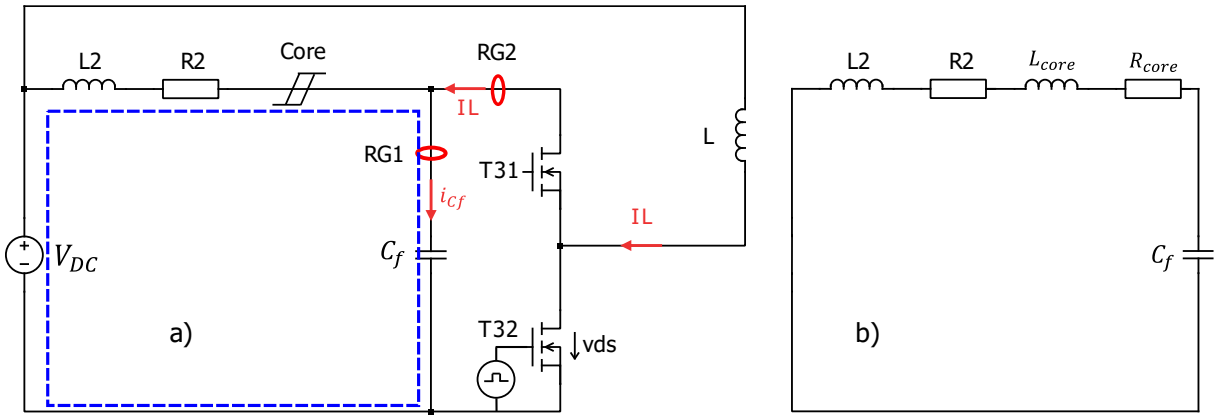


Figure 3.11: *Single pulse test setup to measure the differential inductance of the ferrite core under DC bias excitation current. a) schematic of the test setup, blue dashed line is the resonance circuit. b) the equivalent circuit of the resonant circuit.*

With f_{osc} is the frequency of the oscillation which can be measured from the capacitor's current waveform. Figure 3.12 shows the capacitor current waveform after T32 is turned off. The oscillation begins with large amplitude which is distorted by a big minor BH loop ($\mu_\Delta \neq constant$). The oscillation is then attenuated by the loop's resistance. When the amplitude reaches the small signal region (green dashed line in Figure 3.12), it is no longer distorted ($\mu_\Delta = constant$). The resonance frequency f_{osc} of the current in this region can be used to calculate the core's differential inductance. Measurements will be taken at multiple operating points of the load current. In the roll off region, more measurements should be made to capture the rapid transition of the core's inductance.

Because the load current is small in the weak saturation and a part of the roll-off regions, it is difficult to measure the core's inductance precisely. It is possible to assume that the core's inductance in those regions are equal to the nominal inductance L_0.

In order to illustrate the measurement technique, three distinct cores with varying saturation field strengths (H_s) are evaluated. To ensure the comparison results remain

unaffected by the core's geometry, a compensation factor of 0.52 is applied to the measurements of core FE893, as it has different core dimension. The measurement results are displayed in Figure 3.13. It can be seen that if the core has lower saturation current (Table 3.3), the transition from high to low inductance state is sharper. Moreover, the inductance transition also depends on the core's dimensions. A small diameter core has a sharper transition than a large diameter one.

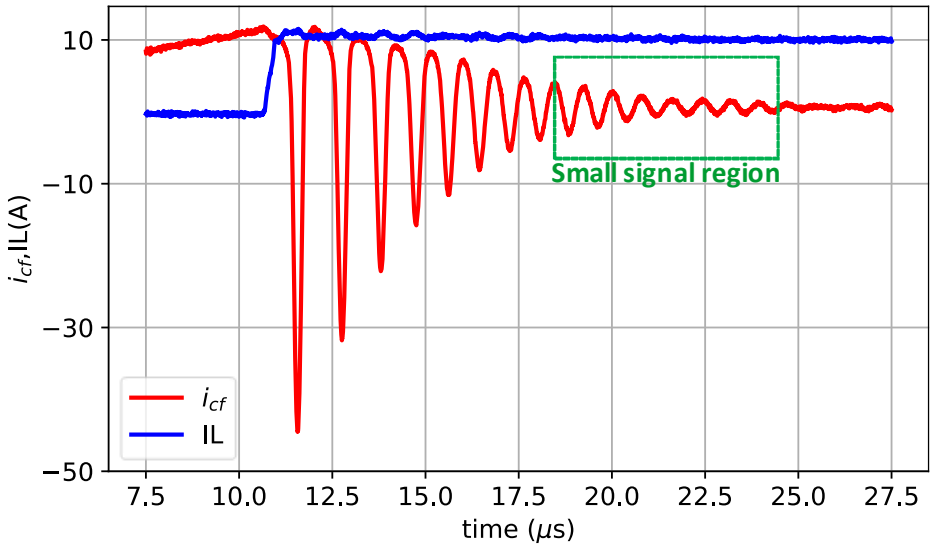


Figure 3.12: *Capacitor's current (red line) and load current (blue line) waveform during single pulse test.*

Table 3.3: *Three different cores are used in the single pulse test to measure the core's differential inductance.*

Serial Number	Material	L_0(nH)	Hs(A/m)	Size ODxIDxL(mm)	Saturation current (A)
B64290L0638X087	N87 MnZn	1340	1200	22.1x13.7x6.35	67
B64290L0638X035	T35 MnZn	3200	325	22.1x13.7x6.35	18
2353289311	FE893 iron powder	128	30000	21.5x12x10	1578

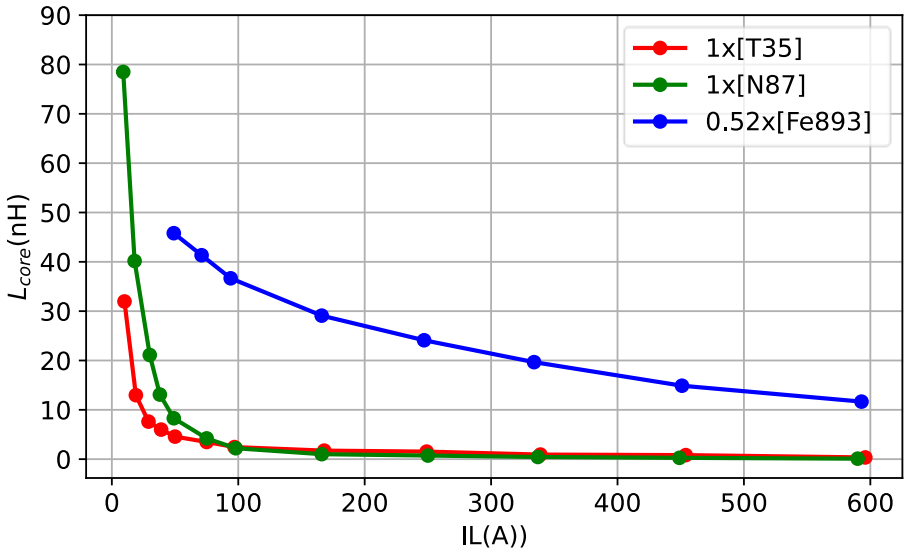


Figure 3.13: *The differential inductance of different magnetic core measured at 25°C in roll-off and deep saturation region.*

3.2.6 Core losses and the oscillation damping

The losses within a ferrite core have various components including hysteresis losses, eddy currents, magnetic domain polarization, and residual magnetism. To simplify the characterization of magnetic material losses, the concept of complex relative permeability is introduced. This parameter comprises a real part $\mu'(f)$ representing the inductive characteristics and an imaginary part $\mu"(f)$ representing the material's resistivity [66]. Both of the real and imaginary of the relative permeability are frequency dependent, which is depicted in Figure 3.14.

$$\mu_r(f) = \mu'(f) - j\mu"(f) \qquad (3.20)$$

The capability of suppression EMC noise depends mostly on the core impedance. According to [67], at high frequency band (radio frequency), the ferrite core's impedance can be modeled as a lumped LCR circuit like in Figure 3.15. The value of R, C, L is a function of frequency. The capacitor value is presented because of the number of turn that the cable is wrapped around the ferrite core [68]. In this application for damping SiC MOSFET switching oscillation, there is only one turn around the ferrite core, so the capacitor value in this case is quite small and neglectable.

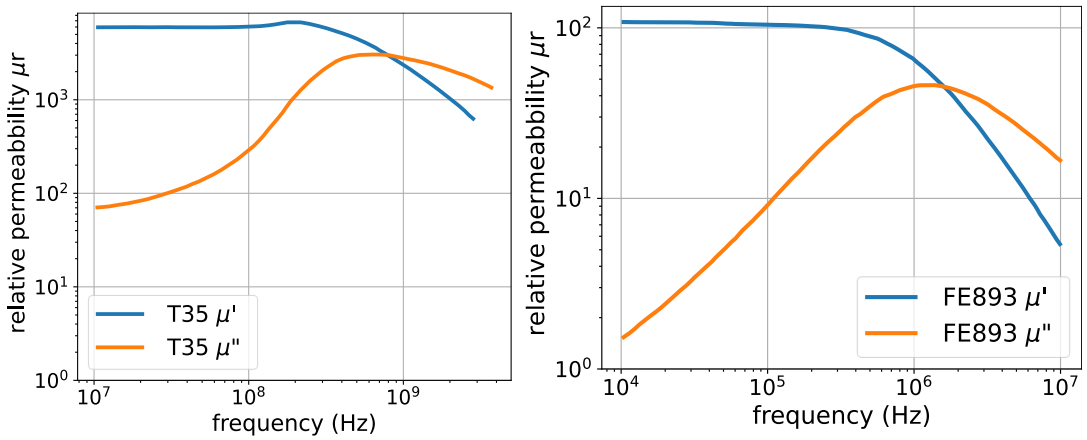


Figure 3.14: *The relative permeability of different magnetic material: soft-ferrite T35 [73], Iron powder Fe893[74].*

If the core is excited at current I and having the core losses P_v, its equivalent resistance can be calculated:

$$R(f) = \frac{2P_v}{I^2} \tag{3.21}$$

In EMI filter applications, there are two common targets: high frequency noise blocking and high frequency noise suppression. To block the high frequency noise, the high impedance ferrites at the noise frequency are used. The noise is blocked to enter the critical components but it is not suppressed. In the noise suppression applications, the high core losses at the noise frequency is preferred.

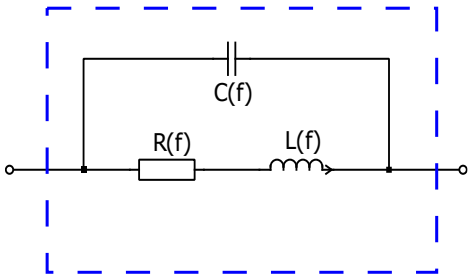


Figure 3.15: *Simplified equivalent circuit of ferrite core in high frequency range.*

3.2.7 SiC MOSFET's clean switching with dual ferrite cores

To demonstrate the high frequency damping of the ferrite cores, the simple 2-level double pulse testbench is set up like in Figure 3.16a. When T32 is turned off, the load current IL will

go through T31 to the upper branch of the circuit, while the resonance current circulates through both upper and lower branch (green dashed line). When T32 is on, the load current will go through T32 to the lower branch of the circuit. Similar to the previous case, the resonance current also circulates through both upper and lower branch (green dashed line). In both cases, while the load current locates either on the upper or on the lower branch of the circuit, the resonance current always circulates through both upper and lower branches of the circuit. The difference in the location between the load current and the resonance current will explain how the dual cores can damp the switching oscillations without saturation at high load current.

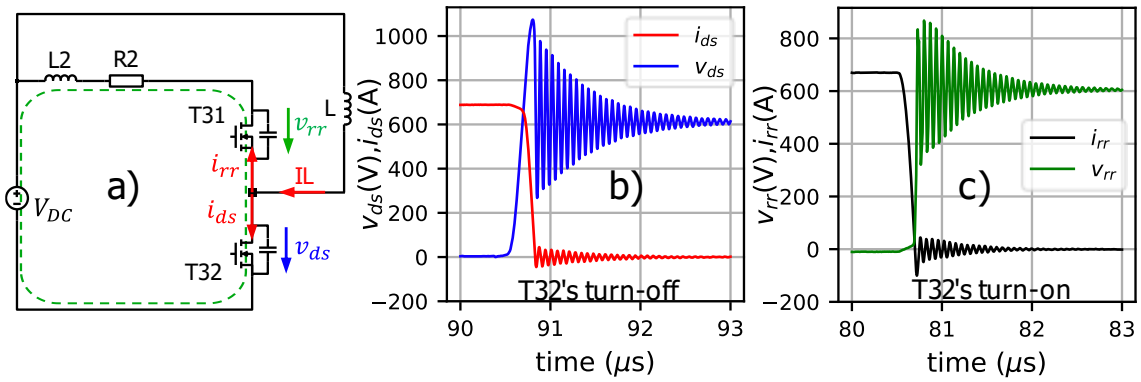


Figure 3.16: *Double pulse test setup: a) without ferrite core, b) T32 is turned off, voltage and current of T32. c)T32 is turned on, voltage and current of T31.*

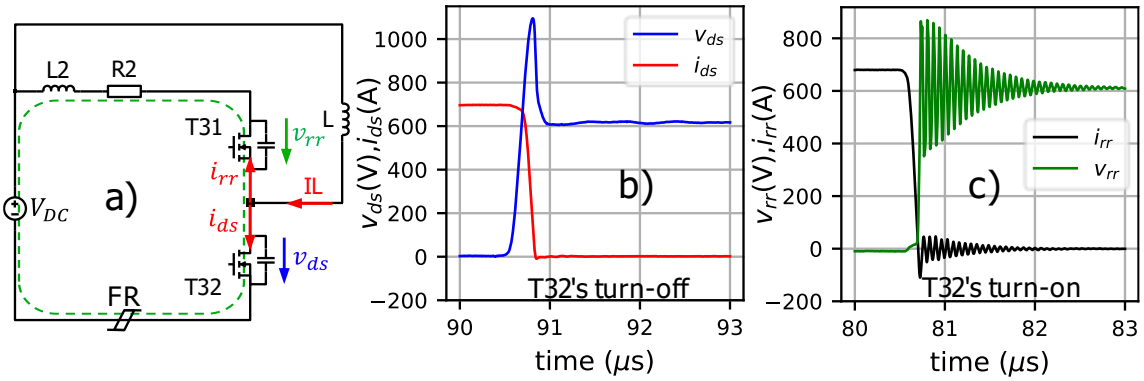


Figure 3.17: *Double pulse test setup: a) with ferrite core FR at -DC terminal, b) T32 is turned off, voltage and current of T32. c)T32 is turned on, voltage and current of T31*

If the ferrite core is installed on the negative terminal of the MOSFET module like in the Figure 3.17a, when T32 is turned on, the load current IL goes to the lower branch and saturates the lower core. Because the resonance current goes through the saturated core, it is not damped and can be seen in Figure 3.17c. If T32 is turned off, the load current IL goes to the upper

branch, the lower core is not saturated in this case. The resonance current circulates through the unsaturated core and it is now damped by the core's losses. The clean voltage and current waveforms are observed in Figure 3.17b.

To damp both of the turn-off and reverse-recovery ringing, the dual ferrite cores are positioned on both positive and negative terminal of the SiC MOSFET module as depicted in Figure 3.18a. Since the load current only saturates one core at a time, while the resonance current circulates through both cores, there is always one unsaturated core to dampen the resonance current. The clean voltage and current waveforms during turn-on and turn-off of T32 are illustrated in Figure 3.18b, c.

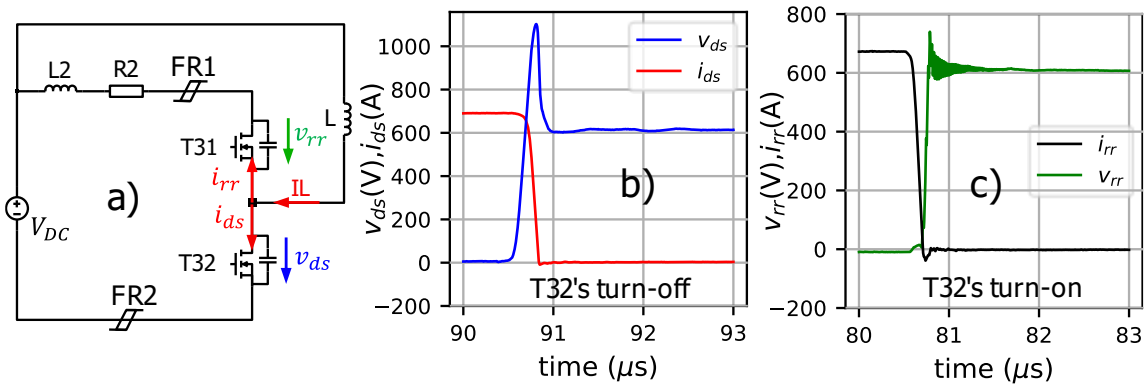


Figure 3.18: *Double pulse test setup: a) with dual ferrite cores FR1, FR2, b) T32 is turned off, voltage and current of T32. c)T32 is turned on, voltage and current of T31.*

3.2.8 Dual cores' behaviors at turn-off

The double pulse test in Figure 3.18a was done with no core, with T35 dual cores (SN B64290L0638X035) and with FE893 dual cores (SN:2353289311). There are some effects that can be observed at the turn-off of T32 in Figure 3.19:

- The turn-off oscillation is damped in different ways: T35 cores damped the oscillation faster than the iron powder Fe893 core.
- The FE893's turn-off overvoltage is very high in compare to T35 and no core cases.
- The di/dt slope in case of FE893 is the slowest. The current slope in case of T35 and no core are very similar.
- It is obvious that Fe893 core has the highest turn-off loss due to the high overvoltage and slow di/dt.

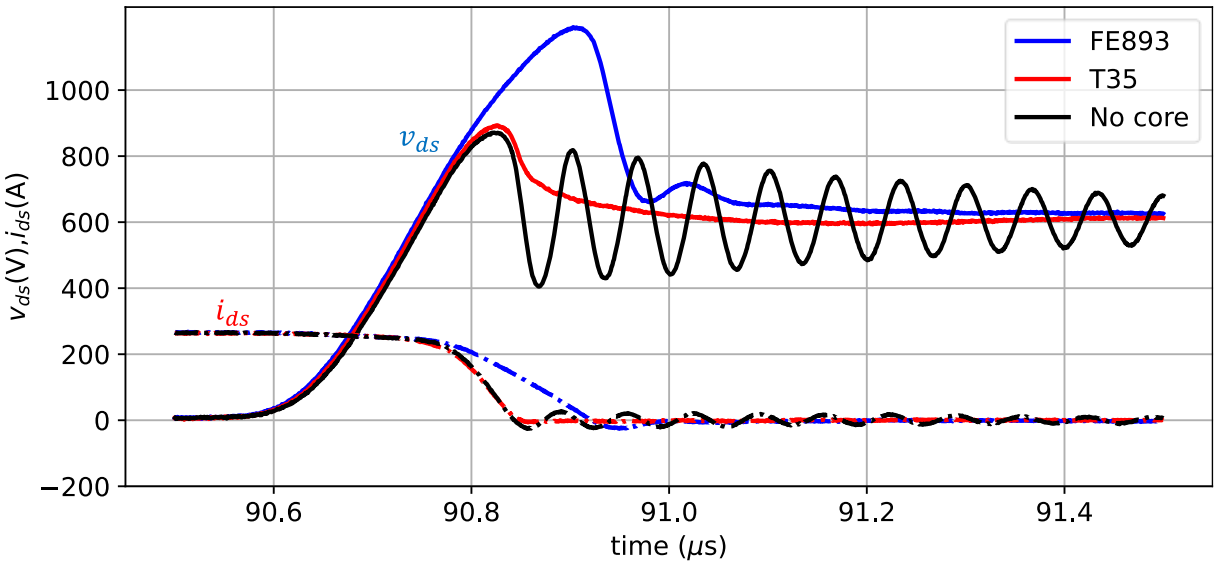


Figure 3.19: *Voltage and current waveform of the lower MOSFET T32 during its turn-off with FE893 core (blue lines), T35 core (red lines), and no core (black lines). Solid lines are voltages, dashed lines are currents.* V_{DC} *= 600V, IL = 250A,* T_j *= 25°C,* R_{goff} *= 18*Ω.

To understand the dual cores' behaviors during turn-off, their differential inductances are plot together with the turn-off waveforms in Figure 3.20. The difference between T35 and FE893 is the total cores' inductances at the peak of the overvoltage (marked with dashed orange lines). Because the FE893 core has a soft transition between the low and high inductance, the upper core and lower core are not completely saturated at the peak voltage moment (Figure 3.20a). The effect leads to high overvoltage. In contrast, T35 core has a sharp transition between the low and high inductance. Therefore, at the peak voltage moment, both cores are completely saturated (Figure 3.20b). The total inductance at that moment is almost equal to the case of no cores are used. The cores' inductances are displayed in Table 3.5.

It can be seen that, at the end of the turn-off (i_{ds} reaches zero), in both cases of T35 and FE893, the inductances of the lower cores return to their nominal values, the upper cores are in deep saturation region. The total cores' inductance $\sum L_{core}$(nH) and the oscillation frequency after turn-off can be estimated by equation (3.22), the result is shown in Table 3.4.

$$f_{osc} = \frac{1}{2\pi\sqrt{(\sum L_{core} + L_2) \cdot C_{oss}}} \qquad (3.22)$$

With $C_{oss} = 2nF$ at 600V, $L_2 = 34\ nH$

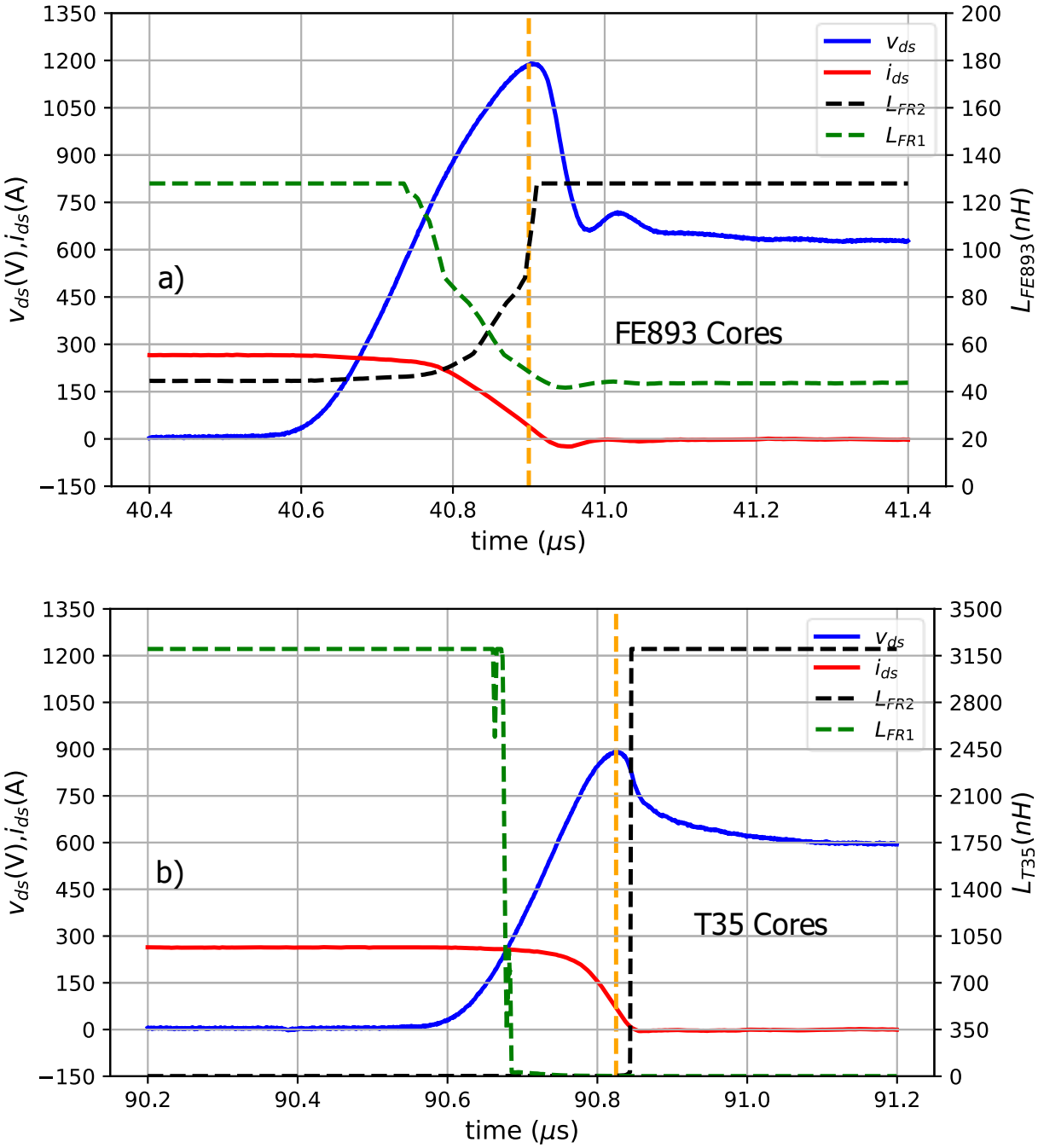


Figure 3.20: *The differential inductance of the upper core (green lines) and the lower core (black lines) during turn-off. a) iron powder core Fe893. b) soft-ferrite T35. V_{DC} = 600V, IL = 250A, T_j = 25°C, R_{goff} = 18Ω.*

Figure 3.21 shows the complex permeability of T35 and Fe893. The $\mu''(f)$ presents the cores' losses. The higher $\mu''(f)$is, the better the damping effect is. It can be seen that, the oscillation frequency of T35 after turn-off is 1.98MHz. According to the datasheet of T35 [73] (Figure 3.21 green dashed line), its $\mu''(f)$ at that frequency is around 2068. In case of FE893,

the oscillation frequency after turn-off is 7.84 MHz, its $\mu''(f)$ at that frequency is 21, according to FE893's datasheet in [74] (Figure 3.21 blue dashed line). It is obvious that the T35 cores' losses are 99 times higher than FE893 cores which explains why its oscillation is better damped.

Table 3.4: *Estimated oscillation frequency at turn-off of Fe893 core and T35 core.*

	T35	Fe893
$\sum L_{core}$(nH)	3202	172
f_{osc}(MHz)	1.98	7.84
$\mu''@f_{osc}$	2068	21

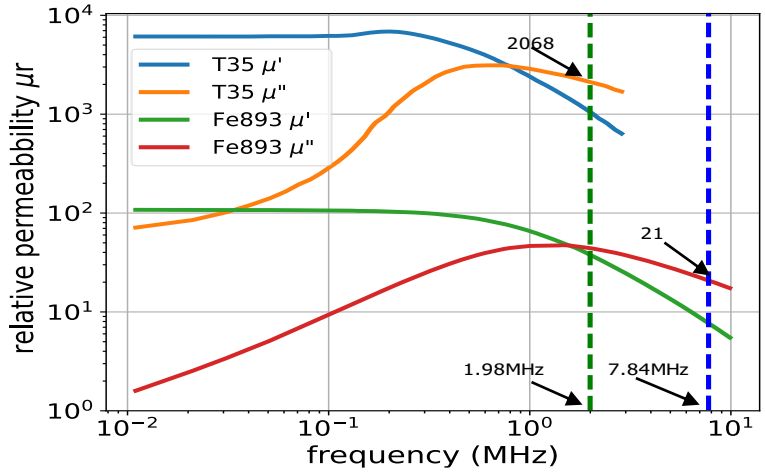


Figure 3.21: *The complex permeability of T35 material and iron powder Fe893 at the turn-off oscillation frequencies [73,74].*

Because of the soft inductance transition, FE893 cores are not completely saturated during the current transient which slows down the current slope. In contrast, T35 cores are completely saturated during the transient. Therefore, its current slope is very near to no core case. It can be concluded that the sharp transition between the high inductance and low inductance of the cores benefits the low turn-off overvoltage and losses.

It is noteworthy that the cores' inductances align closely with the values obtained from the calculation of the overvoltage. For instance: in case Fe893, the overvoltage compares to no core case is 320V, if it is divided by the di/dt, the total core's inductance is 188nH which closely

matches to the measured value at 176nH. In case of T35, the overvoltage compares to no core is 23V and the total core's inductance is 6.7nH which is near to the estimated 4nH (Table 3.5).

Table 3.5: *The upper and lower core's inductance at the overvoltage moment during turn-off.*

	FE893	T35	Nocore
Lcore up(nH)	48	2	0
Lcore low(nH)	128	2	0
Total (nH)	176	4	0
IL(A) @ v_{dspeak}	27	67	70
di_{ds}/dt (A/ns)	-1.7	-3.4	-3.44
V_{dsmax}(V)	1191	894	871

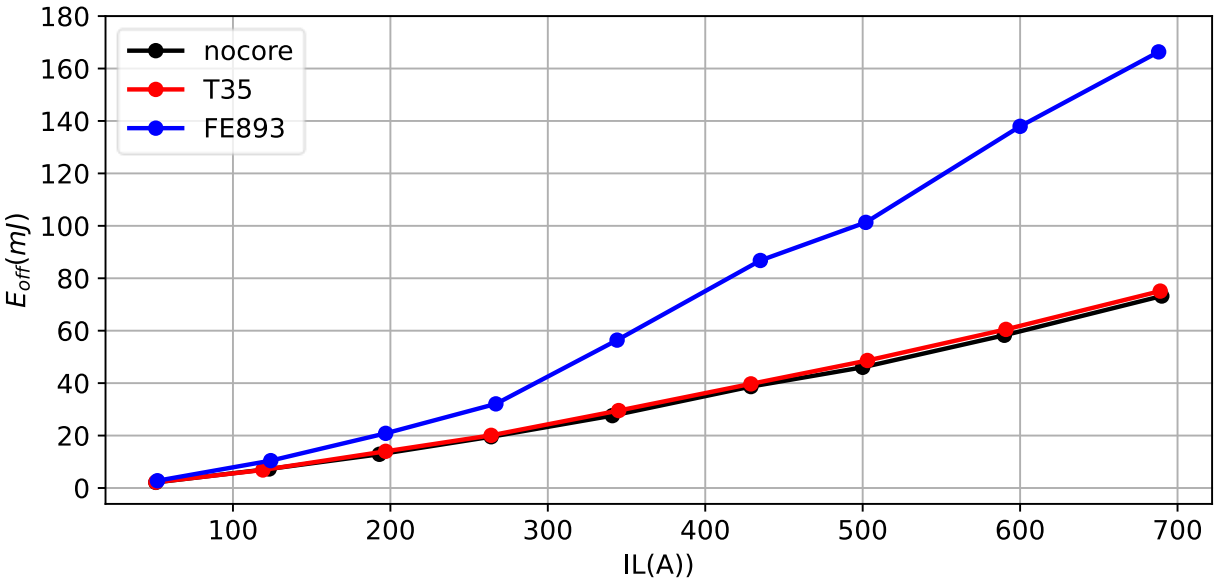


Figure 3.22: *Turn-off losses on SiC MOSFET T32 in three experiment cases. V_{DC} = 600V, T_j = 25°C, R_{goff} = 18Ω.*

Figure 3.22, Figure 3.23 show the turn-off losses and overvoltage on MOSFET T32 at various operating points, the T35 core has slightly higher overvoltage and turn-off losses than the no core case. However, in case of FE893, the overvoltage is tremendously high. When IL >

270A, the active clamping is used to protect the MOSFET. There is no active clamping in case of T35 and no core. The turn-off losses are so high compare to T35 core and no core cases. Therefore, the choice of the correct core's material and dimensions is critical factor in achieving clean switching, low switching losses and reducing overvoltage.

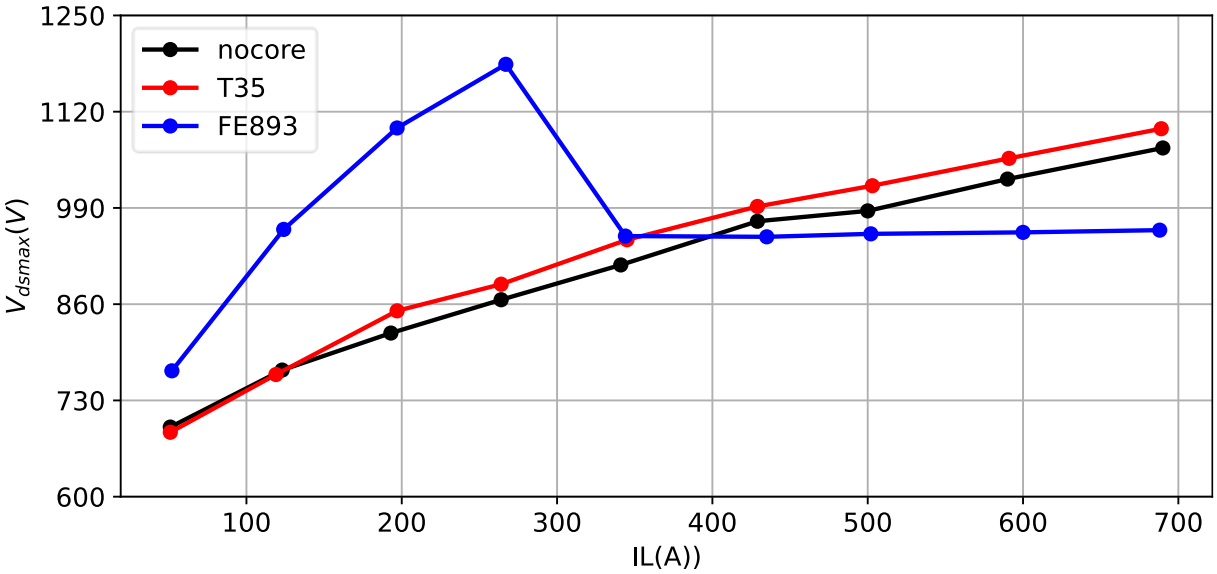


Figure 3.23: *Turn-off overvoltages on SiC MOSFET T32 in three experiment cases. The active clamping is implemented to protect the SiC MOSFET from high overvoltage when IL> 270A only for FE893 cases.* V_{DC} *= 600V,* T_j *= 25°C,* R_{goff} *= 18Ω.*

3.2.9 Dual cores' behaviors at turn-on

Figure 3.24 depicts the voltage and current of the lower MOSFET T32 during its turn-on with Fe893 core (blue lines) and T35 core (red lines) and no core (black lines). There are two effects can be observed:

- When cores are used, there is higher voltage drop during di/dt phase.

- The currents' rising are delayed when cores are used.

To understand the dual cores' behaviors at turn-on, both cores' inductances are plotted with the turn-on waveforms like Figure 3.25. Notably, the initially high inductance of the lower cores contributes to a faster drop in the voltage (v_{ds}) during the di/dt phase and it also delays the flow of current through them. A beneficial consequence of the high cores' inductance at

beginning of the turn-on phase is the reduction of turn-on losses. This favorable impact of ferrite cores on reducing turn-on losses aligns with findings reported in references [90,91].

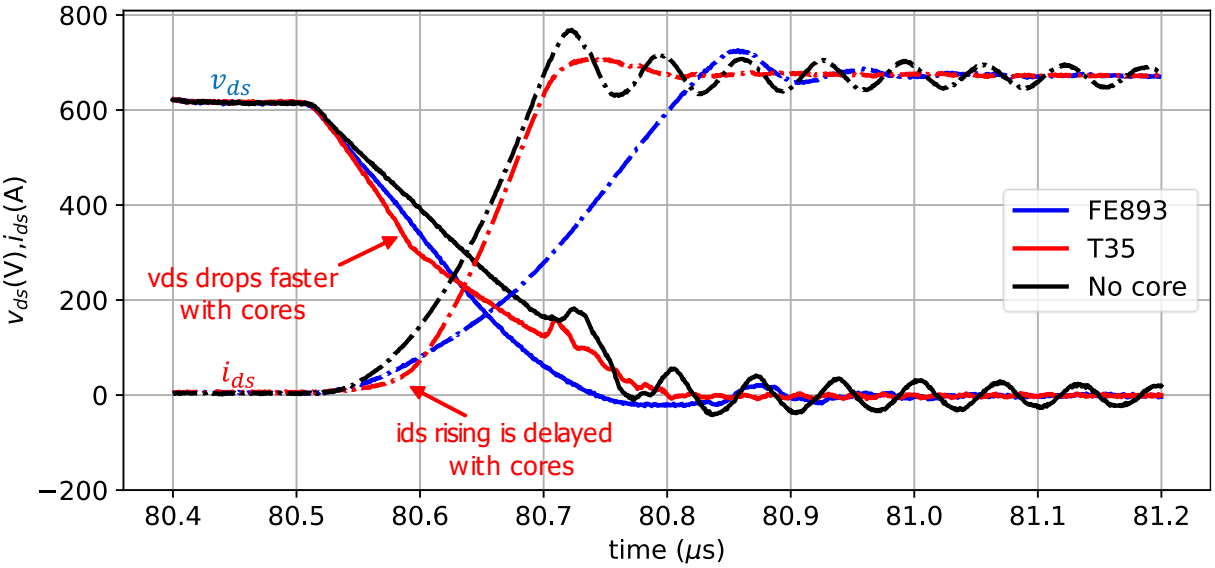
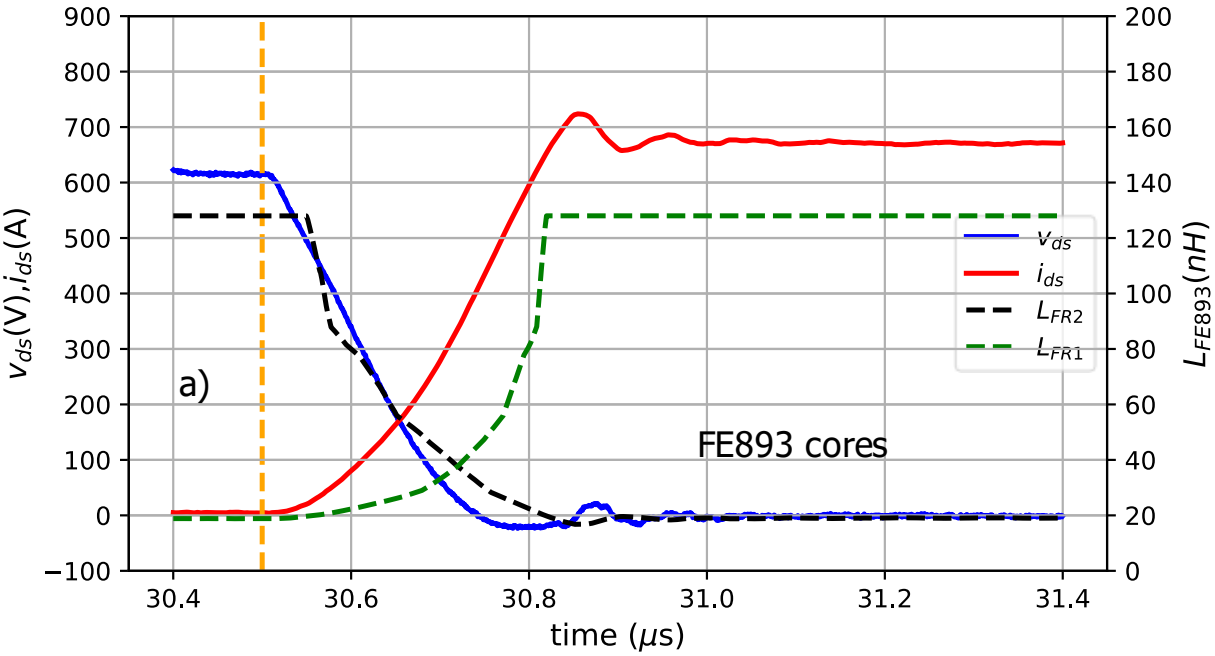


Figure 3.24: *Voltage and current waveform of the lower MOSFET T32 during its turn-on with FE893 core (blue lines), T35 core (red lines), and no core (black lines). Solid lines are voltages, dashed lines are currents.* $V_{DC} = 600V$, $IL = 660A$, $T_j = 25°C$, $R_{gon} = 5\Omega$.



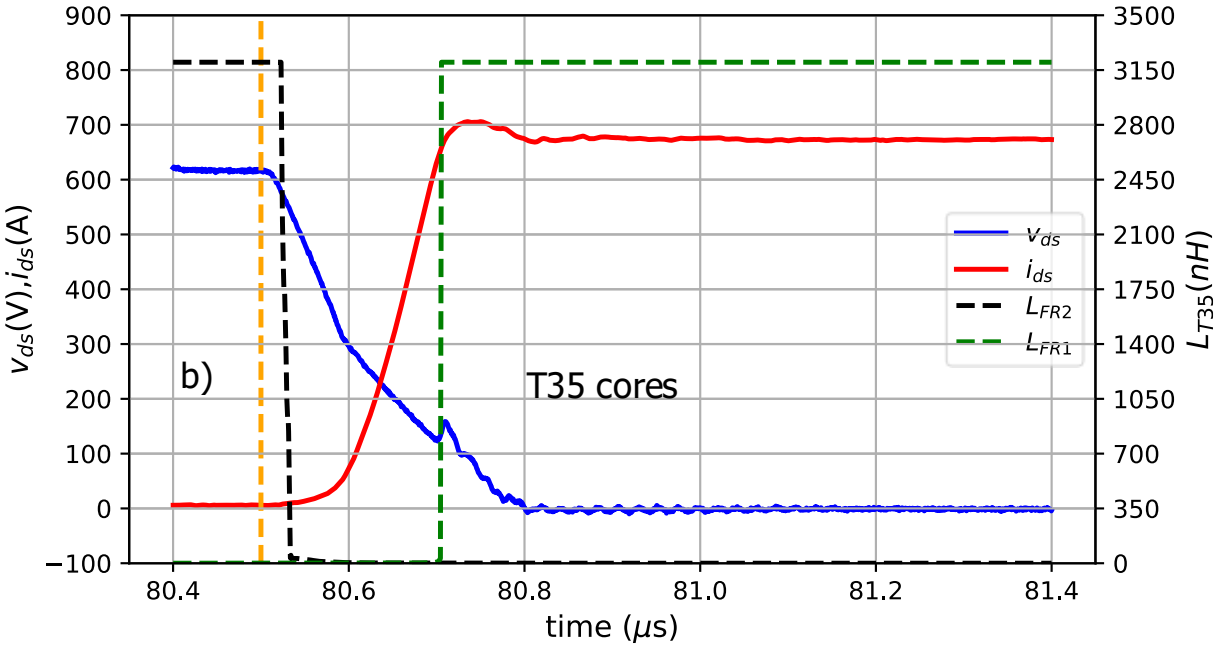


Figure 3.25: *The differential inductance of the upper and lower core during turn-on. a) iron powder core Fe893. b) soft-ferrite MnZn T35. The orange dashed line marks the time v_{ds} starts dropping.*

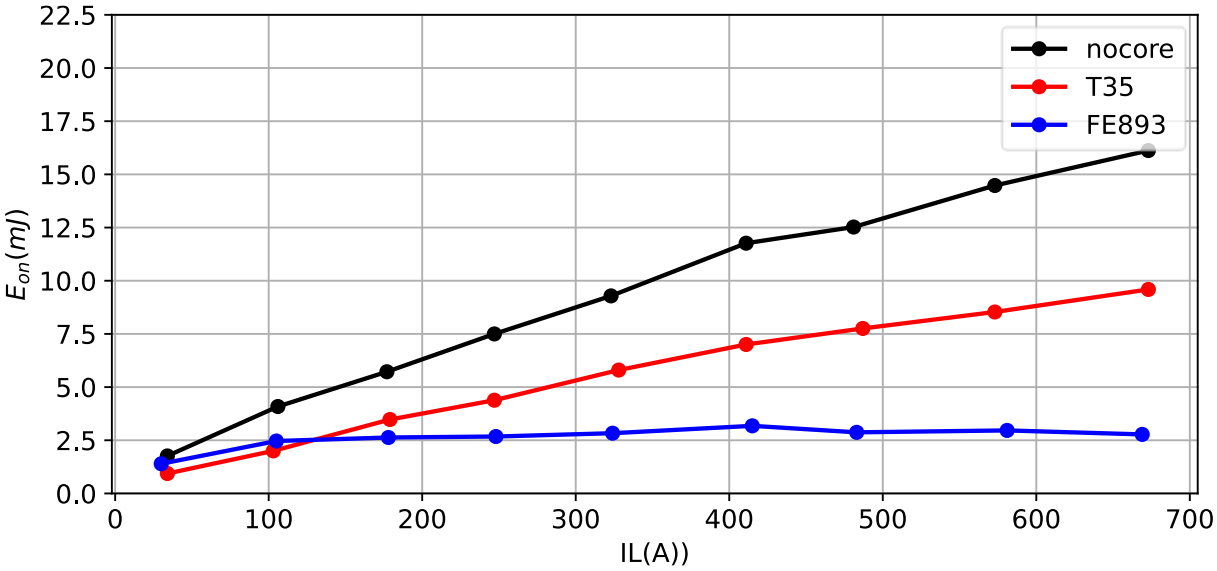


Figure 3.26: *Turn-on losses on SiC MOSFET T32 in three experiment cases. V_{DC} = 600V, T_j = 25°C, R_{gon} = 5Ω.*

Due to the larger initial inductance of the T35 lower core, the voltage drops (v_{ds}) occurs more rapidly, and the di/dt is slower during the initial stages of turn-on. However, it's important to note that the T35 core saturates at a lower current level than the FE893 core. Consequently,

as the load current reaches a certain threshold, both T35 cores become fully saturated, the voltage and current return to their normal state, like the scenario with no core.

In the case of FE893, the lower core is not fully saturated, and the upper core's inductance increases due to the reduction in load current of the upper branch. This effect contributes to a more profound reduction in the v_{ds} voltage and a deceleration in the current flow (i_{ds}). As a result, the turn-on losses are the lowest among the three cases, as depicted in Figure 3.26. It can be concluded that the soft transition between the low and high inductance of the core benefit the turn-on losses due to the higher voltage drop and the delayed current rising slope.

3.2.10 Dual cores' behaviors at reverse-recovery

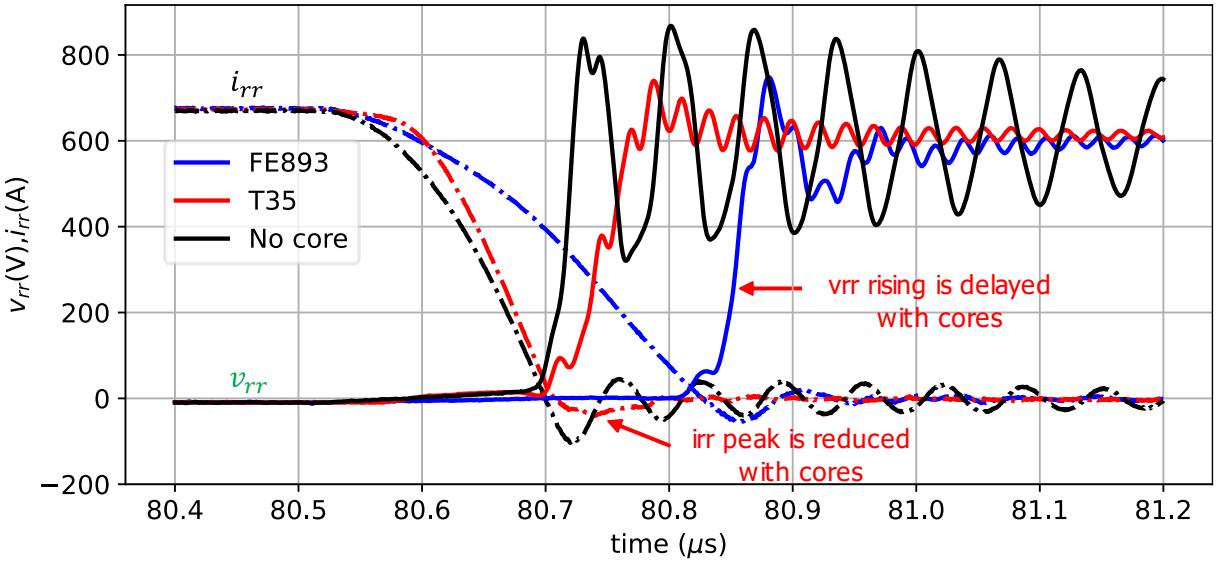


Figure 3.27: *Voltage and current waveforms of the upper MOSFET during its body diode's reverse recovery with FE893 core (blue lines), T35 core (red lines), and no core (black lines). Solid lines are voltages, dashed lines are currents.* V_{DC} *= 600V, IL = 660A,* T_j *= 25°C,* R_{gon} *= 5Ω.*

Figure 3.27 shows the reverse-recovery waveform of T31's body diode during the turn-on of T32, there are 4 visual effects:

- The oscillation amplitudes are significantly reduced in case of T35 and FE893.
- The voltage across the body diode v_{rr} rising is delayed due to the turn-on current is delayed which is described in the last section.

- The current overshoot in case of T35 and FE893 are lower than no core.
- The recovery current slopes in case of T35 and FE893 are softer than no core.

The oscillation is damped by the cores' losses which is mentioned in the turn-off section.

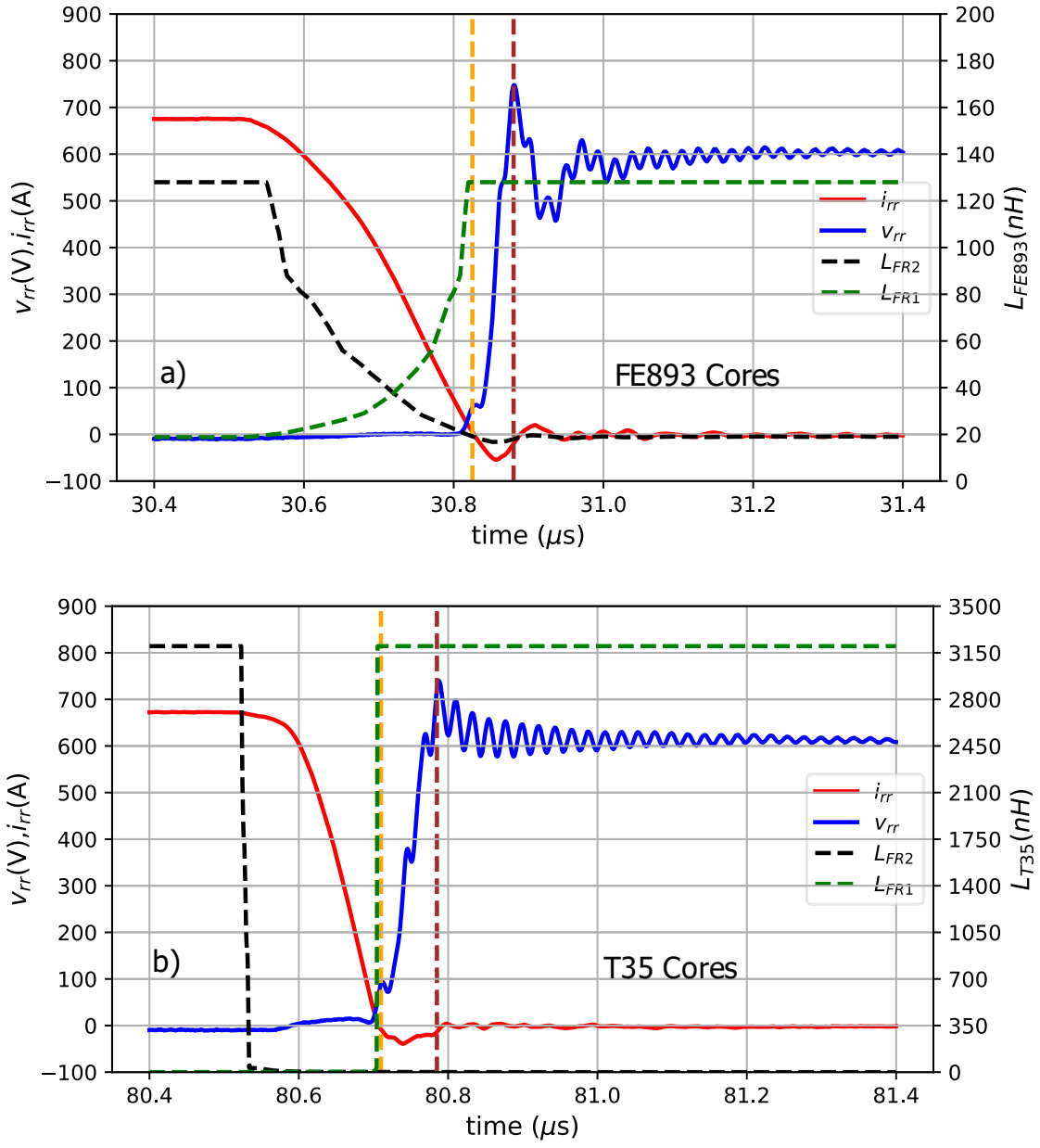


Figure 3.28: *The differential inductance of the upper and lower core during turn-on. a) iron powder core Fe893. b) soft-ferrite MnZn T35. The orange dashed lines mark the time the reverse-recovery starts, the brown dashed lines mark the reverse-recovery current slope.*

It can be seen in Figure 3.28, the dashed orange lines mark the beginning of the reverse-recovery process. At that moment, upper core inductance returns to its highest value. The high

inductance prevents the reverse current flow freely back to the source. The effect reduces the current overshoot and softer the body diode's recovery current slope. The positive effect of ferrite cores on the reverse-recovery behavior is also reported in [92].

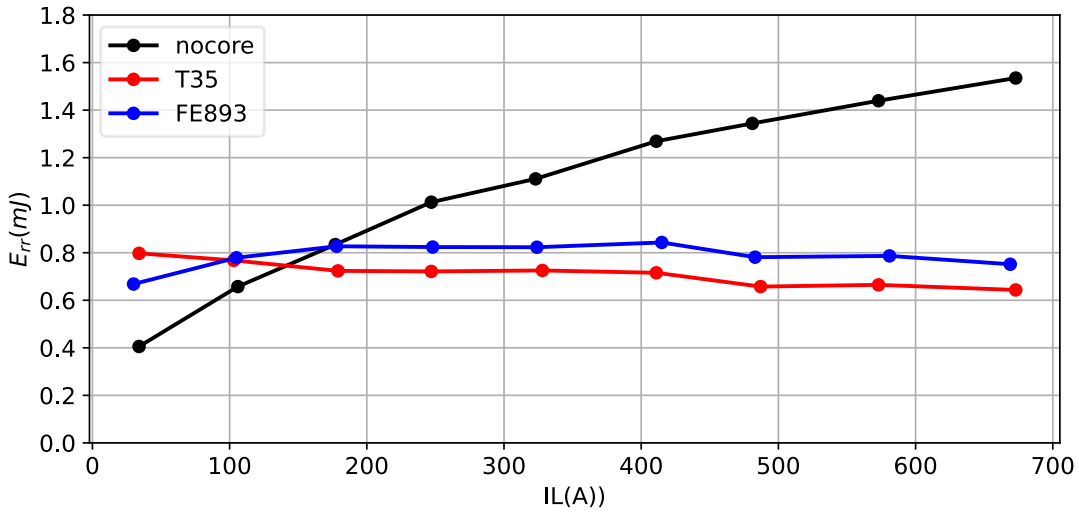


Figure 3.29: *Reverse-recovery losses on T31's body diode in three experiment cases.* V_{DC} *= 600V,* T_j *= 25°C,* R_{gon} *= 5Ω.*

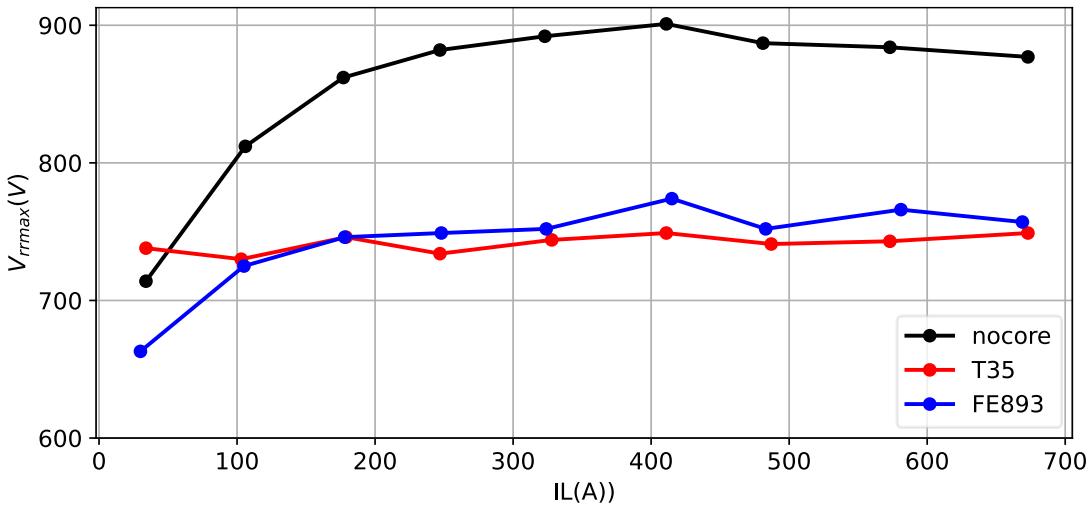


Figure 3.30: *Reverse-recovery overvoltage on T31's body diode in three experiment cases.* V_{DC} *= 600V,* T_j *= 25°C,* R_{gon} *= 5Ω.*

The T35 and FE893 can reduces the reverse-recovery losses lower than the conventional no cores switching which can be seen in Figure 3.29. Because T35 core has larger initial inductance than FE893 core, it reduces more overshoot current. When the cores are used, the oscillation is damped and the reverse-recovery current slope di_r/dt is softer. Consequently, the

overvoltage is also significantly reduced (Figure 3.30). It is possible to increase the turn-on speed to further reduce turn-on losses.

3.2.11 Dual cores' behaviors at low load current

At a low load current, it is insufficient to saturate both of the ferrite cores at the turn-off transient, the total loop inductance at this point is the sum of inductance of two cores and the inductance of the commutation loop. Despite the high inductance in the loop, the overvoltage becomes negligible due to the smaller di/dt associated with low load current. In Figure 3.31, when the MOSFET is turn-off at 50A, the loop inductance is almost double because both of the cores are not saturated at the overvoltage moment. But the di/dt is 15 time smaller than at high load current. The effect results a low overvoltage at low load current.

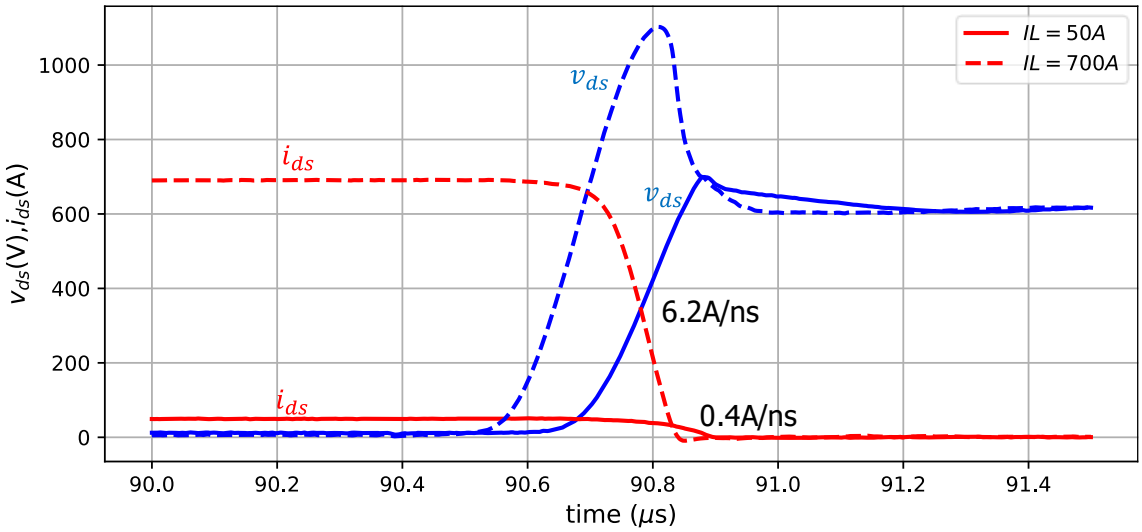


Figure 3.31: *Turn-off voltage and current waveform at IL = 50A and IL = 700A, T35 dual cores.*

Those above experiments demonstrate that ferrite material outperforms iron powder in damping the switching oscillation of a1.2kV- 375A SiC MOSFET.

3.2.12 Core selection

The selection of the ferrite core for damping the switching oscillation should take these flowing properties into consideration:

1. Core's material: The market offers a wide range of soft ferrite materials, each with its own unique composition, Curie temperature, loss characteristics, frequency response, and manufacturing process. The optimal material choice should possess a high imaginary permeability at the resonance frequency. It's important to note that when using cores, the resonance frequency should include the core's inductance, as outlined in Equation (3.22).
2. Core's transition sharpness: The ability to dampen the oscillation without inducing overvoltage at the turn-off depends on the sharpness of the transition between the high inductance and low inductance of the cores. The ability is a combination of the material's softness and core's geometry. The small diameter core has sharper transition than large diameter core with the same material. To evaluate the core's transition sharpness, the measurement method provided in 3.2.5 can be used. Measurements can be conducted for each type of material, regardless of size. Cores made of the same material but differing in ring diameter and length can be easily adjusted by applying the appropriate geometry factor k_g. For ring core, the geometry factor is:

$$k_g \approx \frac{h}{2\pi} ln\left(\frac{r_o}{r_i}\right) \quad (3.23)$$

With h, r_i, r_o are the length, inner and outer diameter of the core. Ideally, the core should return to very low inductance at the turn-off peak voltage. The conventional double pulse test can be performed to verify both damping capability and the turn-off overvoltage at the different operating currents.

3. Core's geometry: the losses in the core typically increase with the core volume. In certain applications, busbar terminals are restricted in length to minimize loop's inductance, thereby limiting the length of the core as well. Shorter cores may lack sufficient resistance to effectively dampen the resonance and have lower core's heat dissipation capability.

In summary, the high frequency oscillation can be damped with the skin-effect capacitor. By selecting suitable material, the conducting plates' high frequency resistance can

significantly increase which help to dissipate the oscillation energy faster. The external plates, in fact, reduce the thermal stress of the capacitor and easily to be cooled.

The dual ferrite cores can be used to effectively damp the high frequency oscillation thanks to the high core's losses in the resonance frequency range. To be able to damp both reverse-recovery and turn-off oscillation, the dual ferrite cores configuration are used. The sharp transition between the high and low core's inductance benefit low turn-off overvoltage. The low turn-on losses and softer reverse-recovery can be archived with high initial core's inductance.

4. Low Frequency Oscillation Damping

4.1 Low frequency oscillation

In the traditional switching approach for 2SiC hybrid ANPC (as outlined in Table 1.4) during the transition from state P to dead time and then to ZP, both IGBTs T11 and T21 remain active (as depicted in Figure 4.1). These two IGBTs establish a closed oscillation circuit, influenced by the stray inductance L_1 and the decoupling capacitor C_f. Specifically, the positive oscillation current flows through IGBT T11 and diode D21, while the negative oscillation current flows through diode D11 and IGBT T21. The low-frequency oscillation circuit is marked by the green dashed lines in Figure 4.1. Upon switching the SiC MOSFETs T31 and T32, their transients trigger both low and high-frequency oscillations. Even after these transients, such as illustrated by the orange line in Figure 4.2, the low-frequency oscillation continues while IGBTs T11 and T21 are still active.

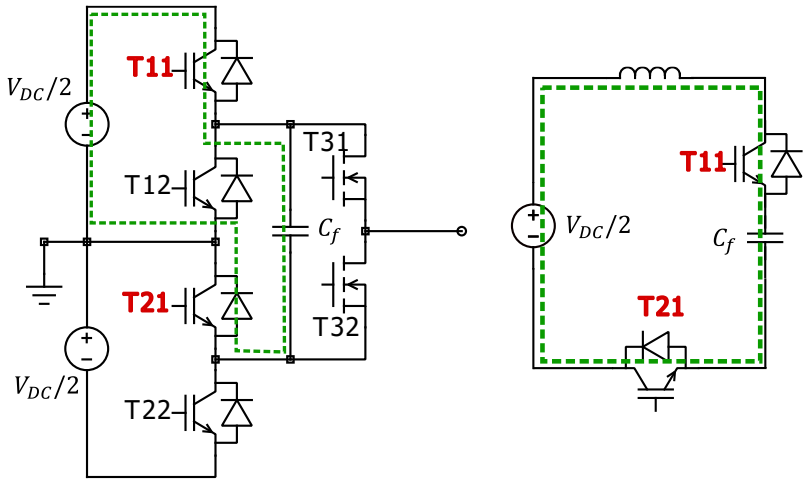


Figure 4.1: *Low frequency oscillation circuit in 2SiC hybrid ANPC. A) the LF circuit (green dashed line) when the ANPC is in its state P and ZP. B) the simplified equivalent LF oscillation circuit.*

To damp the oscillation, Di Zhang suggested to turn off the IGBT and its associated MOSFET which are carrying load current to force load current commutate to other IGBT. Unfortunately, the solution is dependent on load current's direction [26]. In this dissertation,

the special switching states and the safe switching transitions schedule are proposed to actively cut off the low frequency oscillation by turning off one of the IGBT that does not carry the load current. The switching states have the same inverter's output voltage with the conventional switching states and they are independent from the load current's directions. The effect of the active cut-off switching scheme can be seen at the MOSFET's voltage during switching in Figure 4.2.

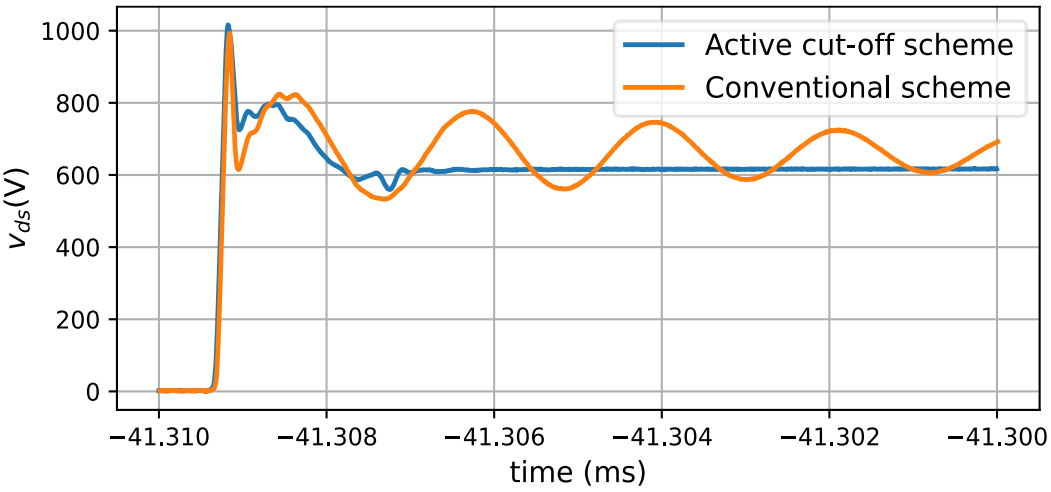


Figure 4.2: *Low frequency oscillation with the conventional switching states (orange line) and the active cut-off switching states (blue line) when the ANPC changes from P to dead time and dead time to ZP.*

4.2 Compare conventional switching states and active cut-off switching states

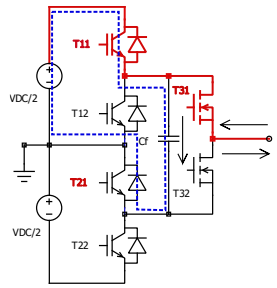
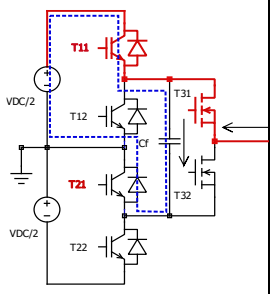
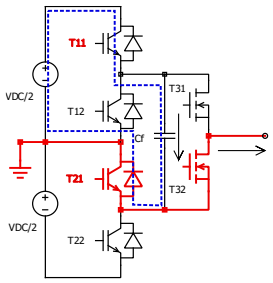
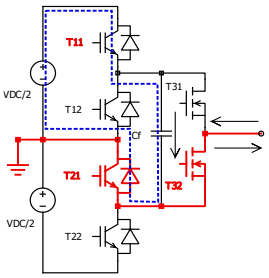
Table 4.1 illustrates the conventional switching states P, ZP and their corresponding dead times. During the transition from state P to dead time, and then to state ZP, as well as vice versa, IGBTs T11 and T21 remain continuously active. The low-frequency oscillation circuit forms a closed loop across all states. The LF resonance current freely flows and maintains the resonance.

Notably, in states P and ZP, the positions of the load current IL are clearly defined by the activated MOSFET, regardless of IL's direction. For instance, if T31 is activated, the load current always passes through T11 and D11, regardless of its direction (positive or negative). Similarly, if T32 is activated, the load current consistently flows through T21 and D11,

independent from its direction. Because at state P, the load current always goes through T11, D11 therefore, T21 can be actively turned off to cut off the resonance circuit without changing the inverter's output voltage.

Only in the dead time state, when both T31, T32 are off, the load current's location is undefined and depends on its direction. If IL > 0, IL goes through T21. If IL < 0, IL goes through D11. To ensure the switching scheme independent from the load current direction during dead time, both IGBTs T11 and T21 are kept active.

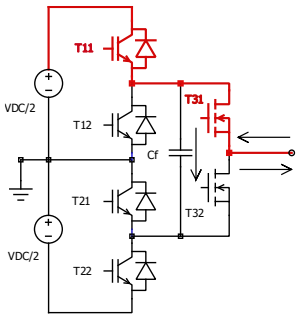
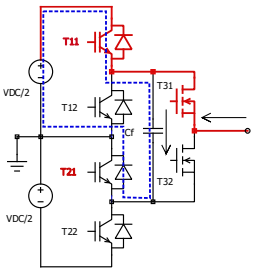
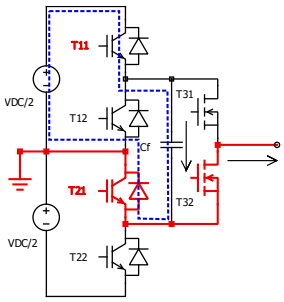
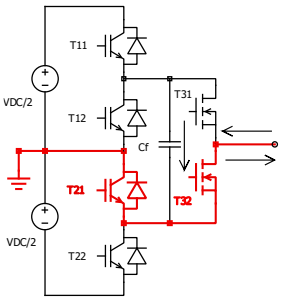
Table 4.1: *Conventional switching state P, dead time, ZP of the hybrid ANPC.*

P2	**Dead time**		**ZP4**
IL < 0; IL > 0	IL < 0	IL > 0	IL < 0; IL > 0
			
T11, T21, T31 are on	T11, T21 are on	T11, T21, are on	T11, T21, T32 are on
$V_{out} = V_{DC}/2$	$V_{out} = V_{DC}/2$	$V_{out} = 0$	$V_{out} = 0$
If T31 is on, IL goes **through T11, D11** in all directions	IL's location is **undefined** and depends on its direction: IL > 0 => IL **through T21** IL < 0 => IL **through D11**		If T32 is on, IL goes **through T21, D21** in all directions
LF: Closed loop	**LF: Closed loop**	**LF: Closed loop**	**LF: Closed loop**

The proposed active cut-off switching scheme concept is outlined in Table 4.2. In contrast to the conventional switching scheme illustrated in Table 4.1, the low frequency (LF) resonance circuit is opened during state P and ZP and only closed for a short period during the dead time. By actively turning off one of the IGBTs that do not carry load current in states P, ZP, N, ZN,

the low-frequency (LF) oscillation is actively cut off, regardless of the load current direction. The switching process details are explained in the following sections.

Table 4.2: *Active cut-off switching state P, dead time, ZP of the hybrid ANPC*

P1	**Dead time**		**ZP1**
IL < 0; IL>0	**IL < 0**	**IL > 0**	**IL < 0; IL>0**
			
T11, T31 are on	T11, T21 are on	T11, T21 are on	T21, T32 are on
$V_{out} = V_{DC}/2$	$V_{out} = V_{DC}/2$	$V_{out} = 0$	$V_{out} = 0$
If T31 is on, IL goes through T11, D11. **T21 can be turned off**	IL's location is undefined and depends on its direction: IL > 0 => IL **through T21** IL < 0 => IL **through D11**		If T32 is on, IL goes through T21, D21. **T11 can be turned off**
LF: Opened loop	**LF: Closed loop**	**LF: Closed loop**	**LF: Opened loop**

4.3 Active cut-off switching states transitions

The Figure 4.3 illustrates 12 potential transitions among the four switching states. These transitions can broadly be categorized into two groups: zero-crossing transitions (depicted by green arrows) and level-crossing transitions (indicated by blue arrows) that switch between $\pm\frac{V_{DC}}{2}$ and zero. In conventional sine-triangle PWM, level-crossing transitions occur at the switching frequency, while zero-crossing transitions occur at the fundamental frequency. It is a common practice in the inverter design that only one switch is changed at a time during the

transition to avoid the shoot-through and the risk of short-circuit faults. Each changing switch in the transition is called step. The more steps the transition has, the longer the transition time is.

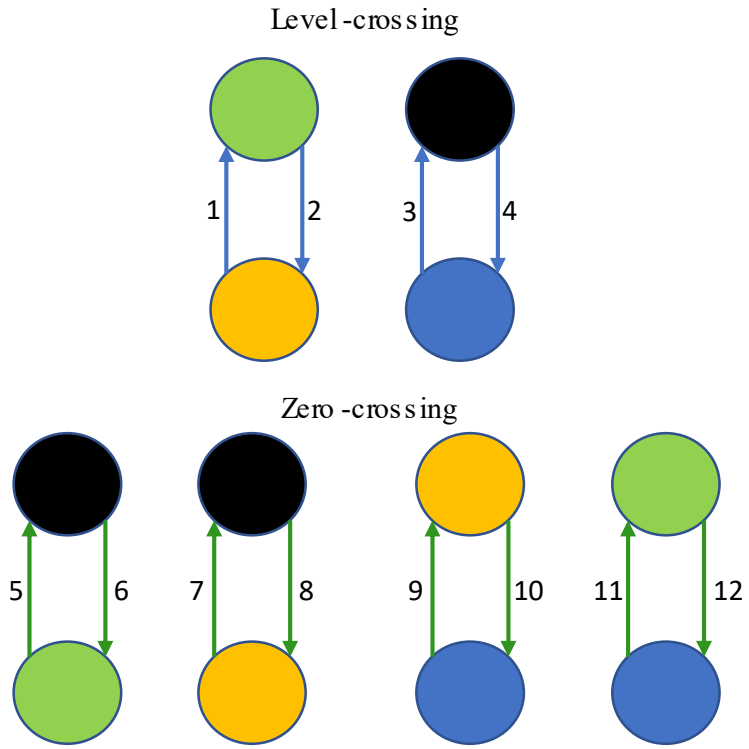


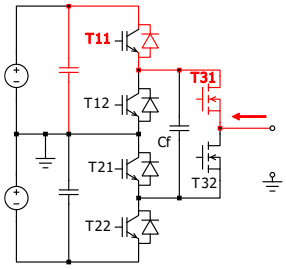
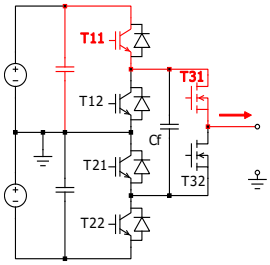
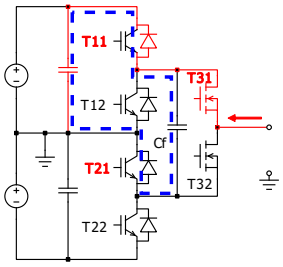
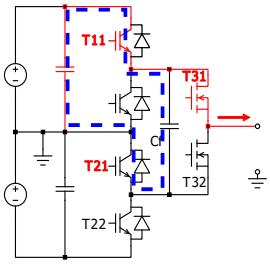
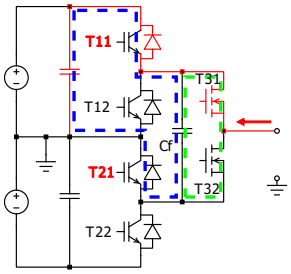
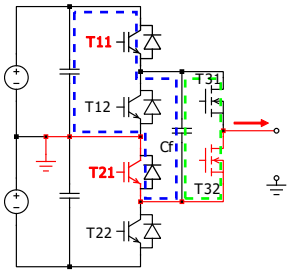
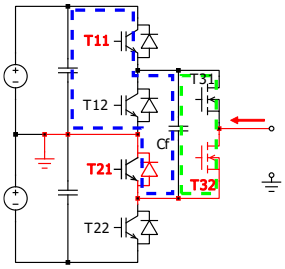
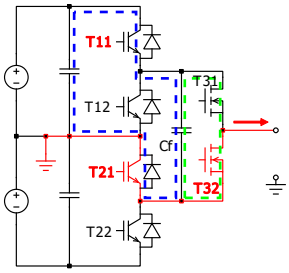
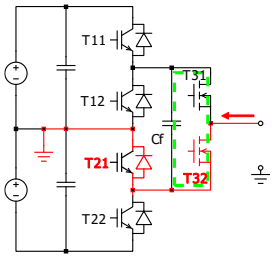
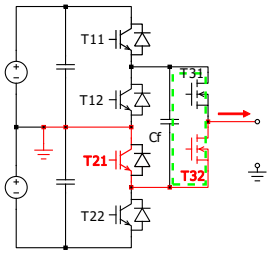
Figure 4.3: *Four switching states of hybrid 2SiC ANPC N, P, ZN, ZP and their 12 potential transitions. The transitions can be divided to level-crossing and zero-crossing groups*

4.3.1 Level-crossing transitions

Table 4.3 outlines the step-by-step transition within level-crossing number 2, moving from state P to ZP with different load current directions. The reverse transition from ZP to P simply involves reversing the steps outlined for the transition from P to ZP.

Figure 4.4 displays the measurement results to demonstrate the effectiveness of the active cut-off switching scheme. Here, the voltage and current of the SiC MOSFET T31 are depicted during the level-crossing transition P ↔ ZP. At the end of the transition from P to ZP, the low-frequency oscillation is intendedly terminated after T11 is deactivated. Notably, there is no observable high-frequency oscillation in this figure due to the utilization of ferrite cores in this experimental setup.

Table 4.3: *Transition number 2, direction from P to ZP.*

Step	IL < 0	IL > 0	Note
1			$V_{out} = V_{DC}/2$. When T31 is on, load current always goes through T11, D11 independently from its direction. No LF oscillation.
2			$V_{out} = V_{DC}/2$. T21 is turned on at no load current. LF loop is closed and starts oscillating.
3			Dead time: T11, T21: on, T31 is off. The HF oscillation is triggered by the T31 turn-off. Load current is on D11 if IL < 0, $V_{out} = V_{DC}/2$, and on T21 if IL > 0, $V_{out} = 0$.
4			$V_{out} = 0$, T32 is turned on. Load current goes through T21, D21 independently from its direction. This step ends when T32 fully conducts
5			$V_{out} = 0$, T11 is turned off at no load current to cut off the LF oscillation. Load current goes through T21, D21.

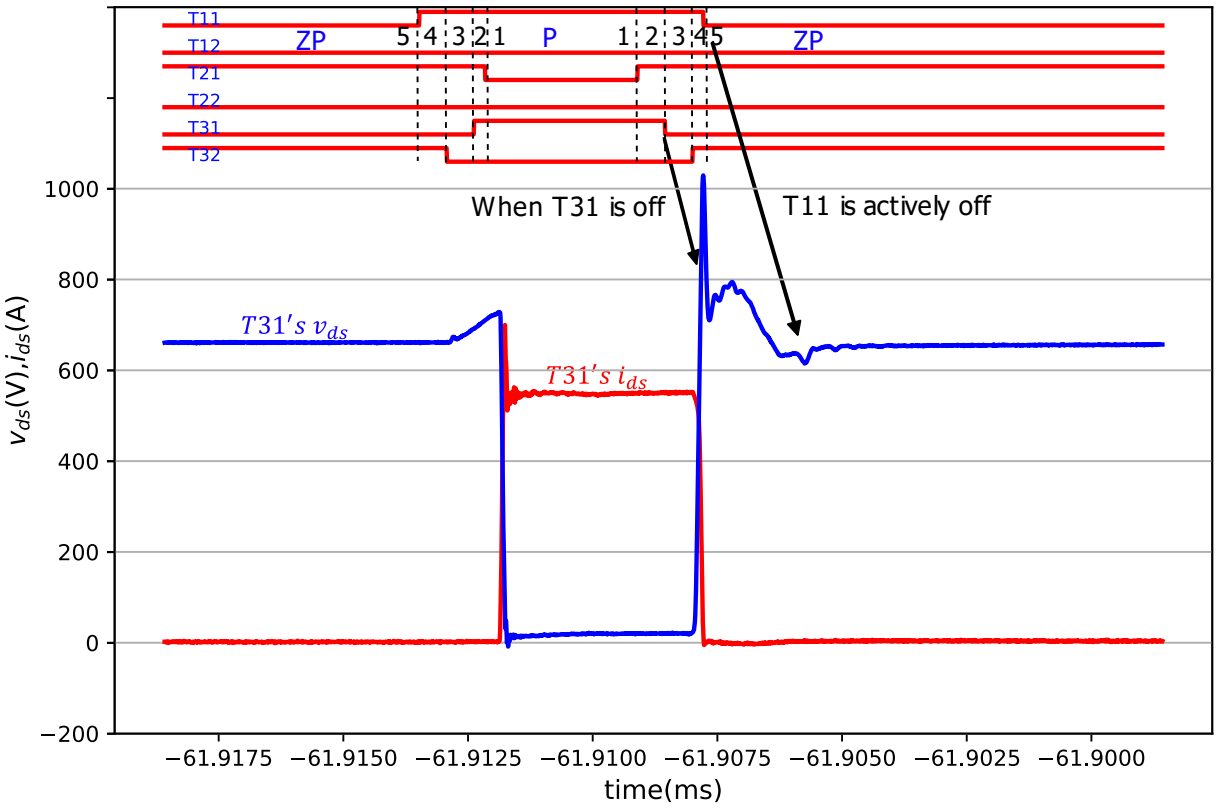
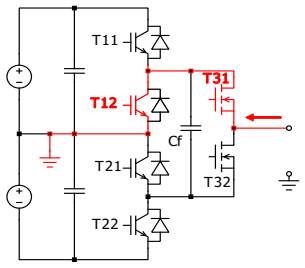
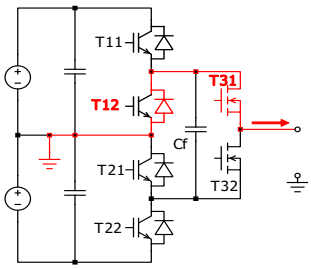
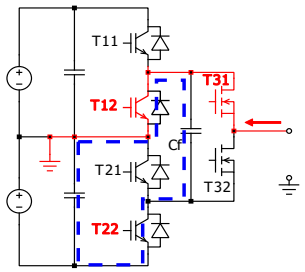
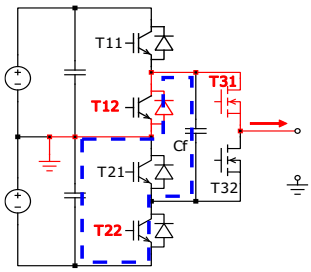
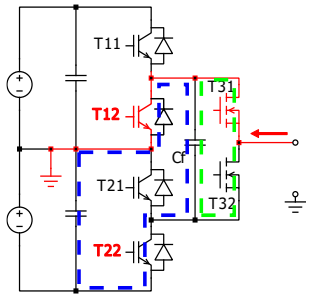
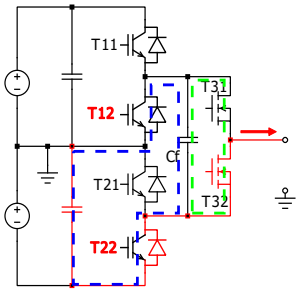
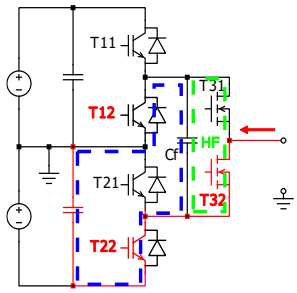
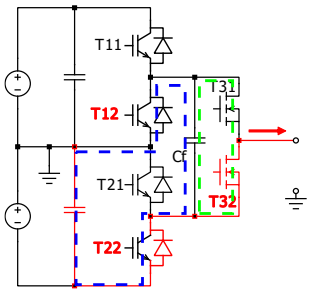
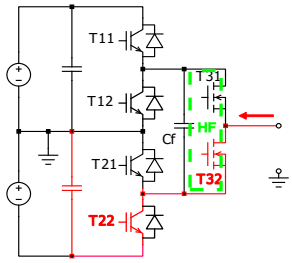
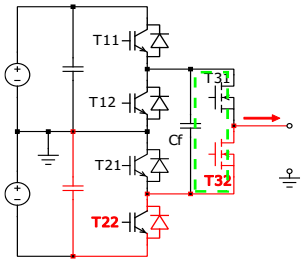


Figure 4.4: *T31's voltage (blue line) and current (red line) waveforms during the level-crossing transitions 1 and 2 between P and ZP when the IL > 0.*

Table 4.4 outlines the level-crossing transition number 3 and 4 between the switching state N, ZN. Additionally, the voltage and current of T31 during the transition is depicted in Figure 4.5. At the end of the transition ZN to N, the low frequency oscillation is effectively cut off when T12 is deactivated.

In this switching scheme, the high frequency oscillation is triggered during the MOSFET switching (step 5th in Table 4.3, Table 4.4, green dashed lines). But it can't be actively cut off by turning off the T31 or T32, akin to the low frequency loop approach. This occurs because the output capacitor of the MOSFET is a part of the HF circuit and exhibits low impedance at the HF resonance frequency. In contrast, the output capacitors of IGBTs have high impedance at the LF frequency. Therefore, when the IGBTs are turned off, the low-frequency oscillation is also terminated. The LF oscillation starts from step 2 and lasts until the end of step 4. The oscillation time depends on the dead time period (step 3) and the SiC MOSFET's turn-on and turn-off time.

Table 4.4: *Transition number 3, direction from ZN to N.*

Step	IL < 0	IL > 0	Note
1			V_{out} = 0. When T31 is on, load current always goes through T12, D12 independently from its direction. No LF oscillation.
2			V_{out} = 0. T22 is turned on at no load current. LF loop is closed and starts oscillating.
3			Dead time: T22, T12: on, T31 is off. The HF oscillation is triggered by the T31 turn-off. Load current on T12 if IL < 0, V_{out} = 0, and on D22 if IL > 0, V_{out} = -V_{DC}/2.
4			V_{out} = -V_{DC}/2, T32 is turned on. Load current goes through T22, D22 independently from its direction
5			V_{out} = -V_{DC}/2, T12 is turned off at no load current to cut off the LF oscillation. Load current goes through T22, D22

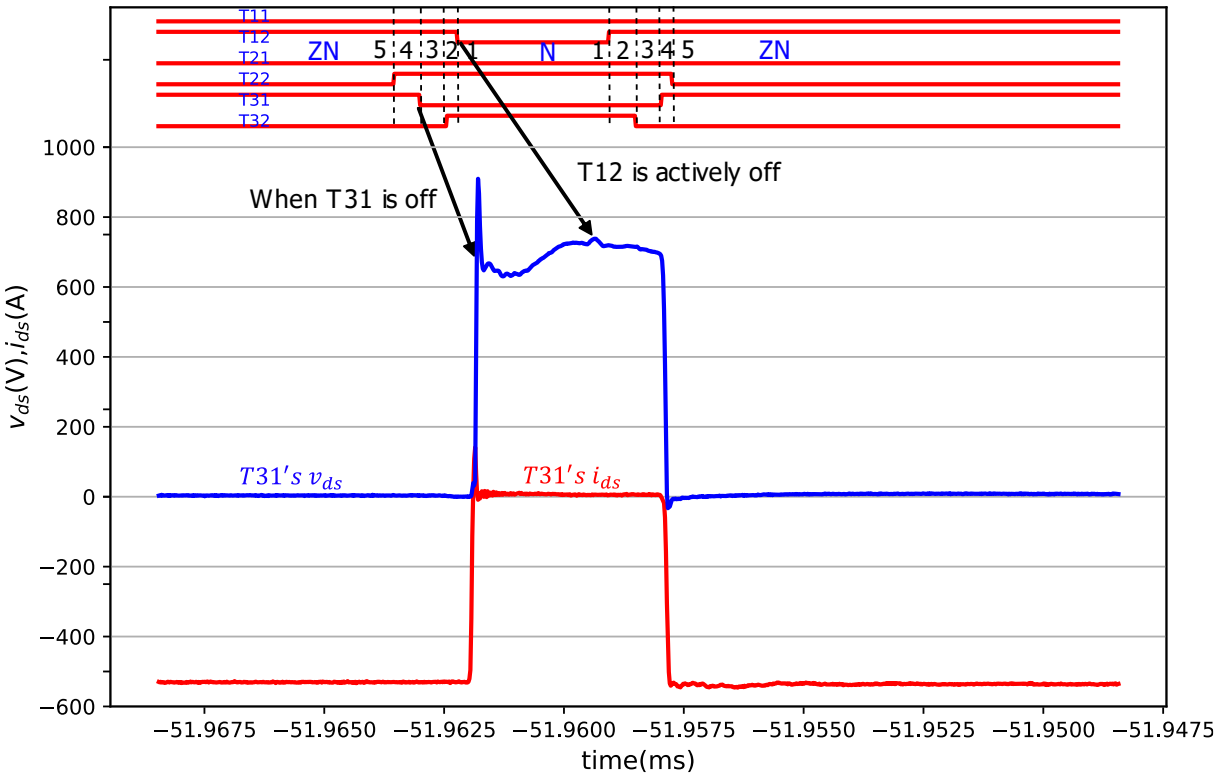


Figure 4.5: *T31's voltage (blue line) and current (red line) waveform during the level-crossing transitions 3 and 4 between N and ZN when the IL < 0.*

Moreover, it is obvious that the IGBTs are switched at the switching frequency in this active cut-off scheme. Since they operate under no load current conditions, there are no switching losses attributed to load current transients. Assuming the decoupling capacitor maintains a constant voltage of $V_{DC}/2$ throughout the transition, the switching losses induced by the low-frequency resonance current can also be ignored.

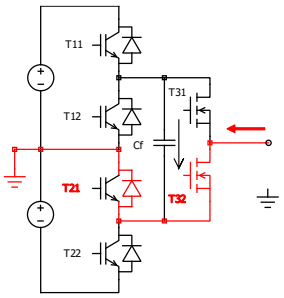
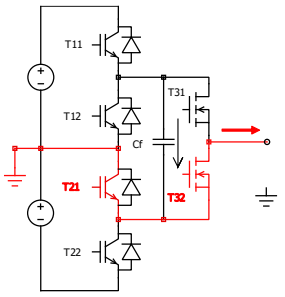
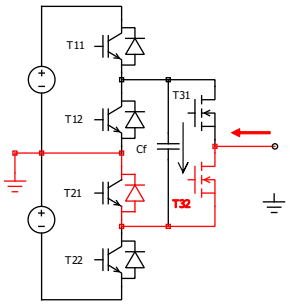
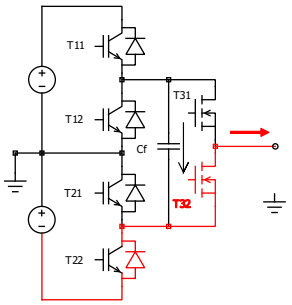
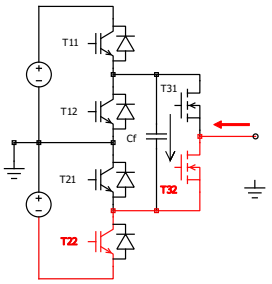
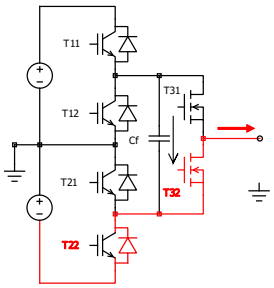
4.3.2 Zero-crossing transitions

In the sine-triangle PWM, depending on the value of the reference signal compare to the carriers' signals, there are 8 possibilities of zero-crossing can happen like in Figure 4.3, the details of those transitions are displayed in Table 4.5 from 5-12.

Transition 5, 6: These direct transitions between P and N without passing through the zero state are irregular transitions that can lead to current spikes due to abrupt changes in output voltage levels. To mitigate this adverse effect, transitions should first pass through the zero states before transitioning to the negative or positive state. For instance, in transition number 5

from P to N, the inverter should transition from P to ZP, then from ZP to N. Transition 5 is substituted with transition 2 followed by transition 7. Similarly, transition 6 is replaced with transition 4 followed by transition 11 in the same manner.

Table 4.5: *Transition number 7, direction from ZP to N.*

Step	IL < 0	IL > 0	Note
1			V_{out} = 0. The inverter is in state ZP
2			T21 is turned off, If IL >0, V_{out} = -V_{DC}/2 If IL <0, V_{out} =0
3			V_{out} = -V_{DC}/2, T22 is on, the inverter is in state N

Transitions 9 and 10: These transitions involve switching between ZN and ZP states. As indicated in Table 4.5, during these transitions, all four switches T11, T12, T21, and T22 completely change their states. The transitions take more time to finish, but the output voltage level remains the same zero volt. In the dissertation, the author proposes to avoid transitions 9 and 10. If a command is given to transition between ZN and ZP, the state machine should remain in its current state and wait for transitions 7, 8, 11, or 12. For instance, if the inverter is presently in the ZP state and receives a command to switch to ZN, it should disregard the

command, stay in the ZP state, and await transition number 7, indicating a transition from ZP to N.

Transition 7, 8, 11, 12: The transition between ZN and P, ZP and N. These transitions happen at fundamental frequency. In those transitions, the MOSFET T31, T32 have the same state and only two IGBTs are switched.

Table 4.5 outlines the steps involved in transition number 7, moving from ZP to N. Due to the open resonance circuit, there is no occurrence of low-frequency oscillation. Additionally, as the MOSFET remains unswitched, there is no presence of high-frequency oscillation. Transition number 8, proceeding from N to ZP, follows the reverse sequence of transition number 7. Similarly, transition number 11, moving from ZN to P, and transition number 12, transitioning from P to ZN, mirror transitions 7 and 8, respectively, owing to the symmetry of the ANPC configuration.

The zero-crossing transition approach which is described in this dissertation shows some advantages compare to the conventional approach:

- Less transition steps so the zero-crossing duration is shorter.
- There is no oscillation triggered during the transition.
- The load current location is always defined and on one side of the ANPC during the transition because one of the MOSFET is always on. If compare to the transition 5, 6 or 9, 10 there are dead time states in the transition (both MOSFET are off) which make the load current location unpredictable. The effect poses a risk to have full DC link voltage on the switching devices.

4.4 Decoupling capacitor's behaviors during the active cut-off transitions

In the active cut-off switching scheme, it is important to understand the decoupling capacitor's behavior during the transition which helps to select the optimal capacitor's value. Because of the symmetrical switching between the level crossing P, ZP and N, ZN, the investigation for the case P, ZP can be applied also for N, ZN transitions. The voltage and current of the decoupling capacitor in one fundamental cycle are displayed in Figure 4.6. The

zoom in the transitions between P and ZP when the load current is positive and negative are displayed on Figure 4.7 and Figure 4.8. In those figures, the blue numbers 1, 2, 3, 4, 5 mark the steps of the transition between P and ZP, the time $t_1, t_2, t_3, t_4, t_5, t_6, t_7, t_8$ present the switching events that change the capacitor's current.

At the beginning of the transition from ZP to P, the inverter is in step 5 and at ZP state, the capacitor C_f is charged to the voltage V_{cf0} (Figure 4.7b and Figure 4.8b). At the time t1, when T21 is closed, LF is triggered and C_f releases its stored energy. The capacitor's voltage and current can be modeled as:

$$i_{cf}(t) = \frac{\frac{V_{DC}}{2} - V_{cf0}}{\sqrt{\frac{L_1}{C_f}}} \cdot \sin(\omega_1 t) \quad (4.1)$$

$$v_{cf}(t) = (V_{cf0} - V_{DC}/2) \cdot \cos(\omega_1 t) + V_{DC}/2 \quad (4.2)$$

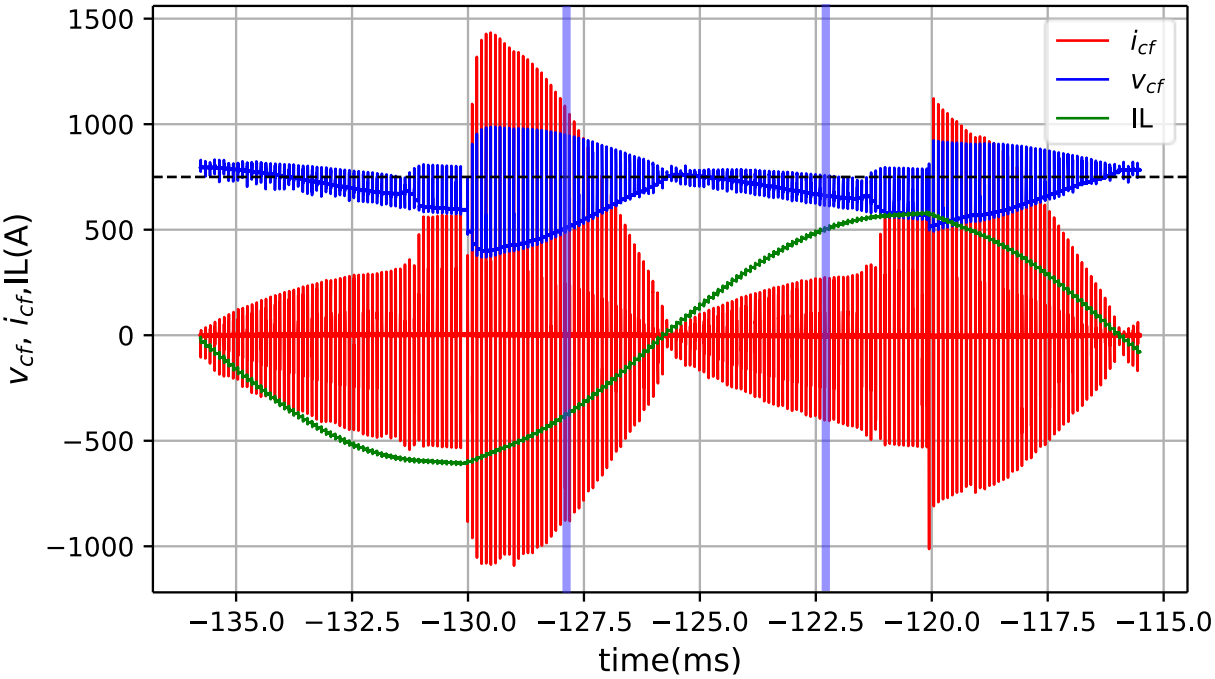


Figure 4.6: *Decoupling capacitor's voltage (blue line) and current (red line) during one fundamental cycle of the load current (green line).*

If $V_{cf0} > V_{DC}/2$, the capacitor is discharged and vice versa. The absolute value of $|V_{cf0} - V_{DC}/2|$ is proportional to the voltage and current oscillation amplitudes. This explains why the capacitor current in Figure 4.8a is larger than in Figure 4.7a after t_1.

In Figure 4.7b, when the inverter changes from step 4 to step 3, T32 is turned off. Because there is no change in the $i_{L1}(t)$ current and $v_{cf}(t)$ between the steps, there is also no change in the oscillation energy. If the inverter changes from step 3 to step 2 when IL > 0, the load current IL changes its location from the neutral branch to the DC+ branch. At the first moment when T31 is on, the load current doesn't flow directly to DC+ branch instead to the capacitor C_f and then to the DC- branch (Figure 4.7b, step 2, dashed green line) because at the current transient, the capacitor path has lower impedance than DC+ branch, the capacitor's current at the moment just after t_2 is $i_{cf}(t_2^+) = -IL$. Consequently, there is current jump -IL in the capacitor current at t_2 which adds more energy to the oscillation. The current slope triggers another oscillation on top of the previous LF oscillation. The oscillation after t_2 can be modeled by the flowing equations:

$$i_{cf}(t) = \frac{\frac{V_{DC}}{2} - V_{cf0}}{\sqrt{\frac{L_1}{C_f}}} \cdot \sin(\omega_1 t) - IL \cdot \cos\big(\omega_1 (t - t_2)\big) \quad (4.3)$$

$$v_{cf}(t) = (V_{cf0} - V_{DC}/2) \cdot \cos(\omega_1 t) - IL \cdot \sqrt{\frac{L_1}{C_f}} \cdot \sin\big(\omega_1 (t - t_2)\big) + V_{DC}/2 \quad (4.4)$$

The current jump can be observed in Figure 4.7a at t_2. There is similar effect when IL < 0 in Figure 4.8b. When the inverter changes from step 4 to step 3, there is a current jump of $i_{cf}(t_2^+) = IL$ at step 3 of Figure 4.8b. At the time t_3, the IGBT T21 is turned off to cut off the oscillation. The capacitor current before t_3 is positive so it goes through T11 and diode D21. When the capacitor's current returns to zero, it enters the reverse-recovery process of D21 between t_3 and t_4 (Figure 4.9). The process is turned over from step 1 back to step 5 when there is a transition from P to ZP which are marked with the times t_5, t_6, t_7, t_8 which have similar behaviors like t_1, t_2, t_3, t_4.

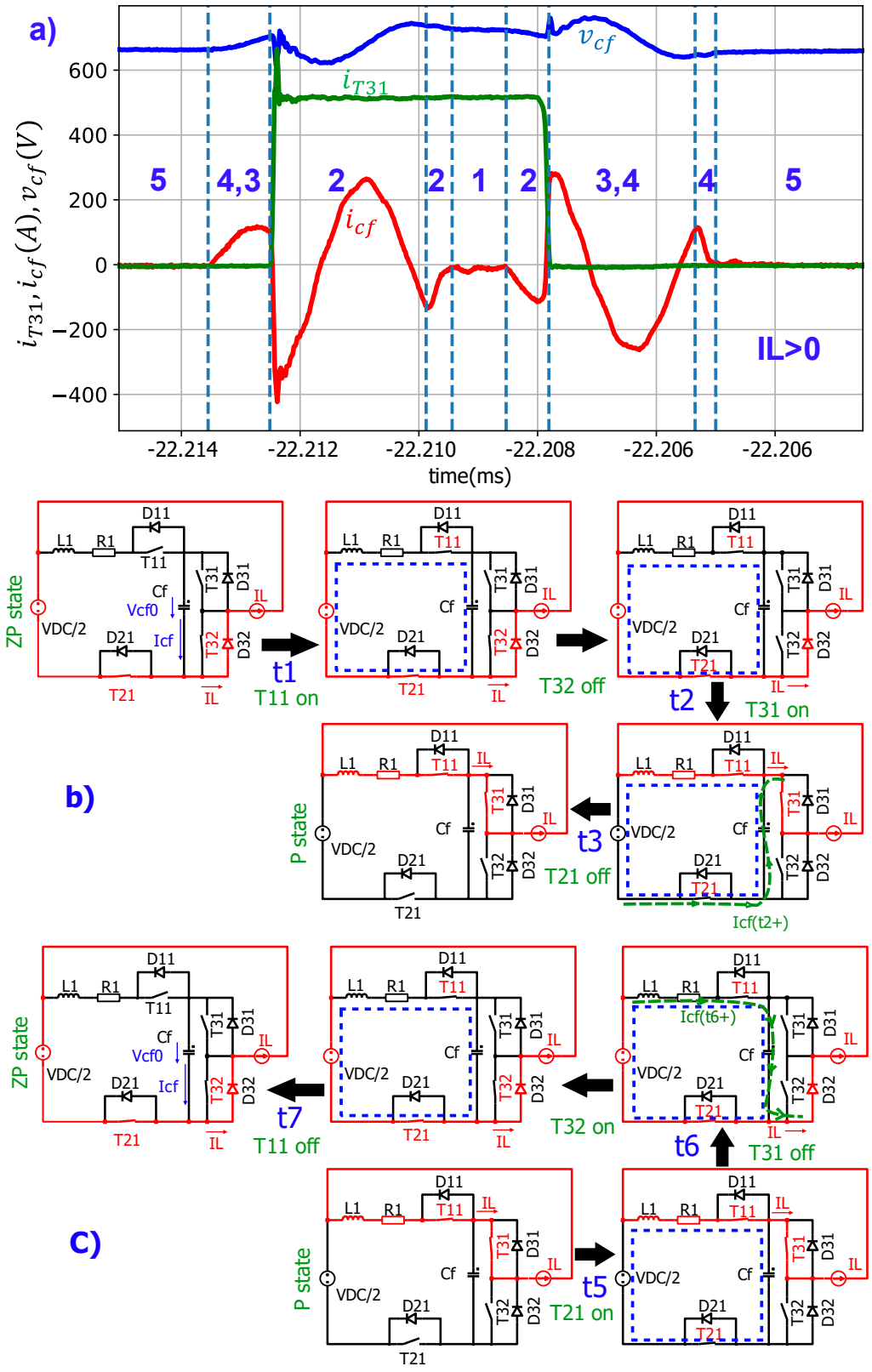


Figure 4.7: *Measurement result: Decoupling capacitor's voltage (blue lines) and current (red lines) during level-crossing transition between P and ZP states when the load current IL > 0.*

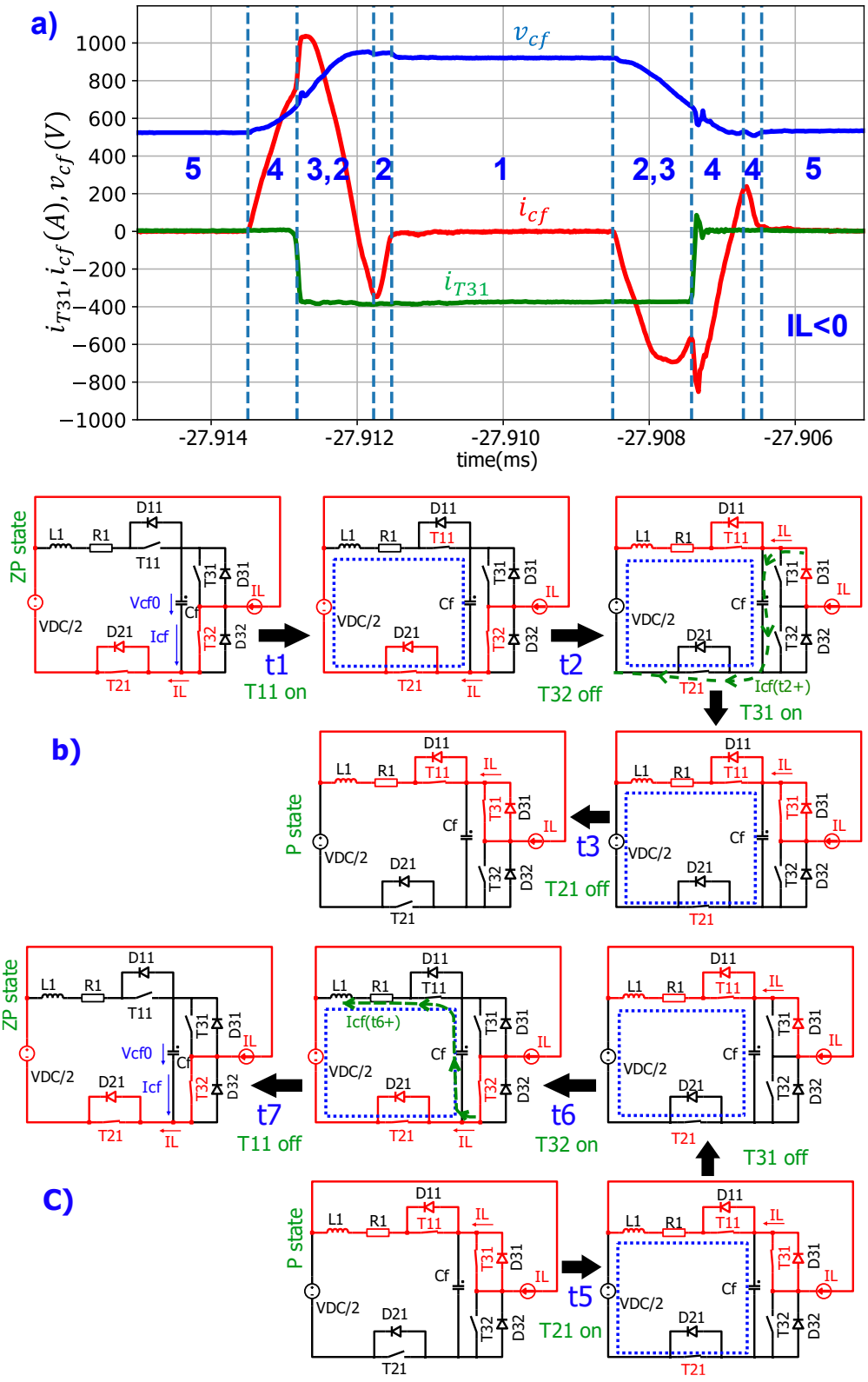


Figure 4.8: *Measurement result: Decoupling capacitor's voltage (blue lines) and current (red lines) during level-crossing transition between P and ZP states when the load current IL < 0.*

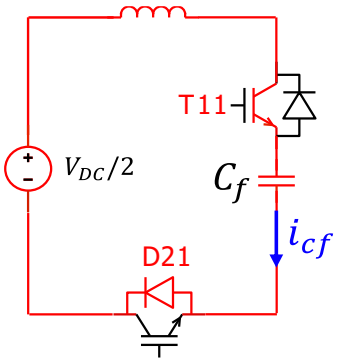


Figure 4.9: *Reverse-recovery process of D21 during t_3 and t_4.*

To verify the behavior of the decoupling capacitor during the transition from step 4 to step 1, a simple PLECS simulation is set up like in Figure 4.10. The initial capacitor voltage V_{cf0} and load current IL are assigned according to the measurement result of IL > 0 and IL < 0 in Figure 4.7a and Figure 4.8a.

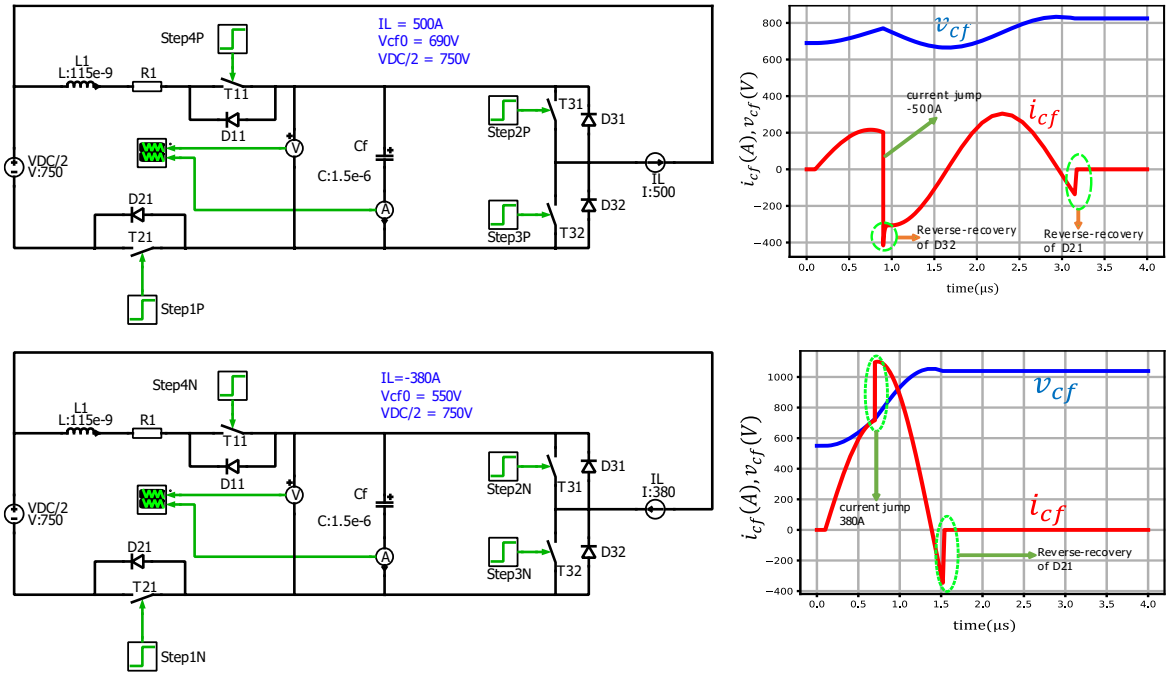


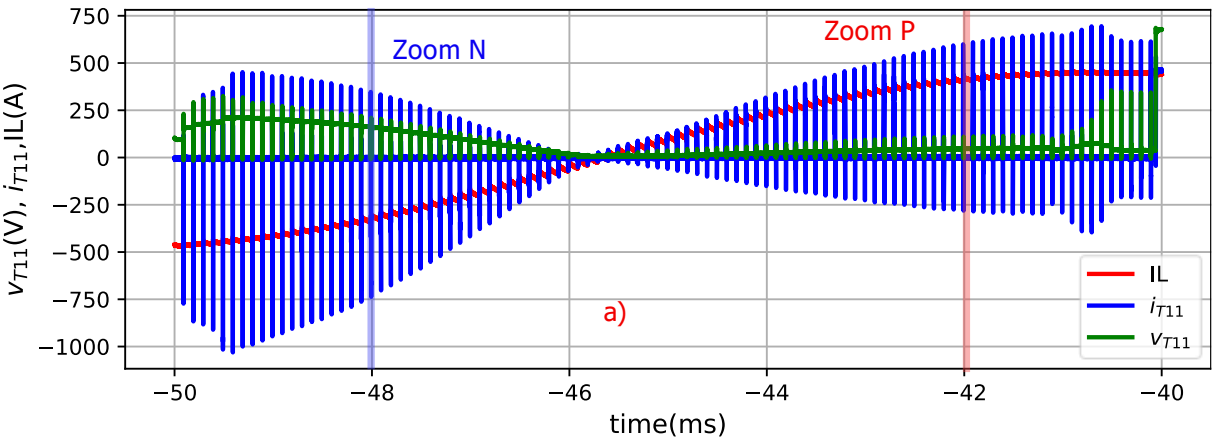
Figure 4.10: *PLECS simulation to verify the transition behavior from step 4 to step 2. Diodes are PLECS's library model with reverse-recovery effect.*

The simulation results show very near to the measurement results for both cases. The capacitor's current jump of -500A can be observed at time 0.9 µs when IL = 500A and a jump of 380A at 0.7 µs when IL = -380A in Figure 4.10. Diode D21 and D32 are the reverse-recovery diodes. The reverse-recovery effects can be seen at t_2, t_3 when IL > 0.

4.5 Decoupling capacitor's voltage drifting

One drawback associated with the active cut-off switching method is that the capacitor's voltage remains floating during the switching phase, because only one of its terminals is directly linked to the DC link. Illustrated in Figure 4.7a and Figure 4.8a, the capacitor current is asymmetrical during the transitions of P→ ZP and ZP → P, causing uneven charging and discharging of the capacitor and thus contributing to voltage fluctuation over time. This asymmetrical behavior arises from current jumps occurring at different times. To illustrate, during the transition from P→ ZP under positive load current (as depicted in Figure 4.7b), the current jump happens at the turn-off of T31. Conversely, during the transition from ZP → P (illustrated in Figure 4.7c), the current jump occurs at the turn-on of T31. Analogously, for transitions like P→ ZP in negative load current (as shown in Figure 4.8b), the current jump emerges at the turn-off of T32. Conversely, during the transition from ZP → P (depicted in Figure 4.8c), the current jump is observed at the turn-on of T32. The difference between turn-on and turn-off delays, along with different transient durations, leads to the initiation of oscillations at different times, subsequently the capacitor charging and discharging are not equal.

The voltage drift, in fact, leads to switching losses on the IGBT. This becomes evident at step number 4, as seen in Figure 4.7a and Figure 4.7b, when IGBT T11 is on. If the capacitor is completely charged to $V_{DC}/2$, no voltage drop occurs across the IGBT, resulting in no loss. However, if the capacitor voltage deviates from $V_{DC}/2$, the voltage drop across T11 together with the oscillating current generates turn-on losses in T11. The same situation happens at step 1 when T21 is off to cut off the oscillation. The effect can be observed on the Figure 4.11.



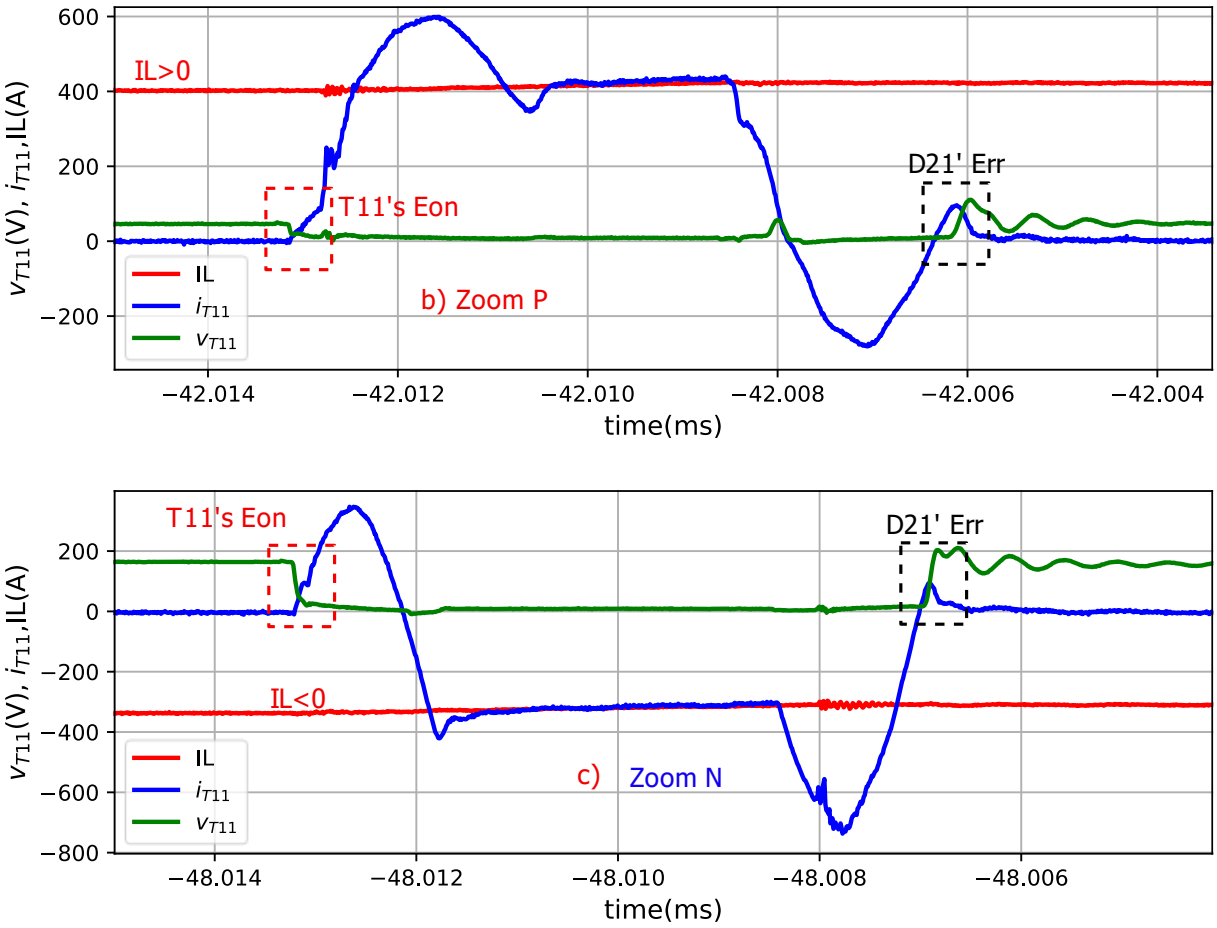


Figure 4.11: *Drifting voltage of the decoupling capacitor and the switching losses on IGBT. a) during the level crossing transition P, ZP,* $v_{T11} = \frac{V_{DC}}{2} - v_{cf}$. *b) when IL > 0, c) when IL < 0.*

4.6 Switching transitions time optimization.

Within the active cut-off switching scheme, the duration of the level-crossing transition is considerably longer compared to the traditional switching approach. This long transition period imposes limitations on the shortest available turn-on, turn-off times at very high or very low modulation indices, leading to load current distortion at the peaks and zeros of the output voltage (refer to Figure 4.12, Figure 4.13 and Figure 4.14). Due to the short transition time, the conventional switching scheme has lower current distortion than the active cut-off scheme, especially at low modulation index, which is illustrated in Figure 4.13, Figure 4.14 and Figure 4.15.

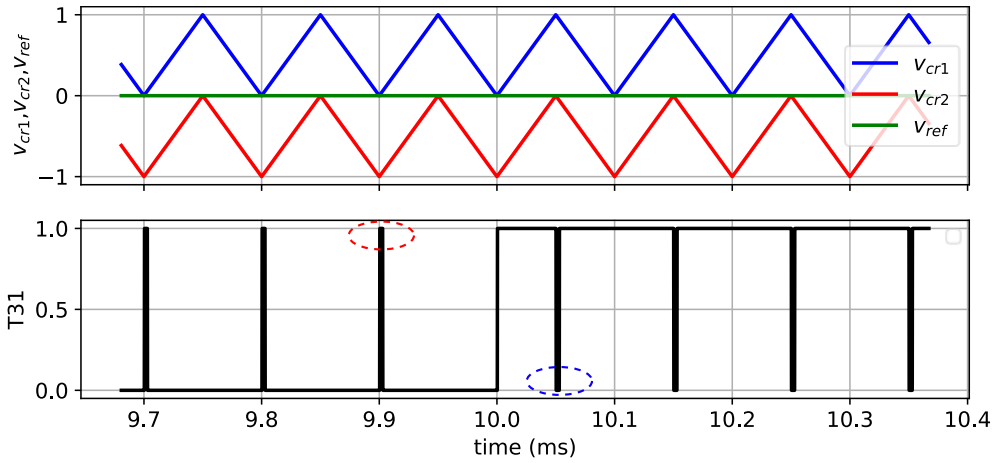


Figure 4.12: *The smallest turn-on and turn-off time during the switching at very small modulation index.*

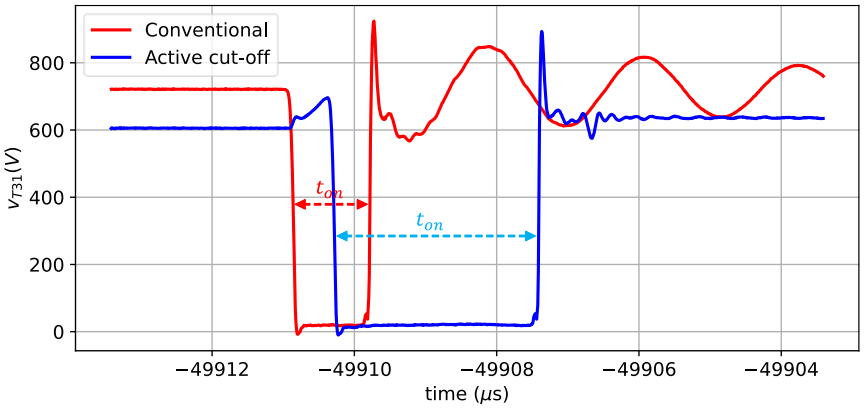


Figure 4.13: *Compare the shortest available t_{on} time between the conventional switching scheme (dashed red arrow) and the active cut-off (dashed blue arrow). The voltage across T31 during P, ZP transitions at IL = 450A.*

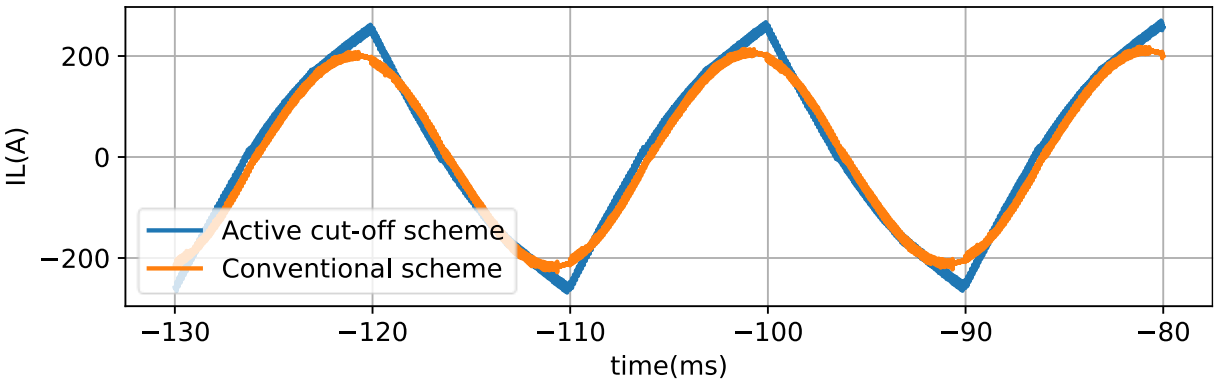


Figure 4.14: *Load current waveform at the same modulation index = 0.03 when using conventional and active cut-off switching scheme.*

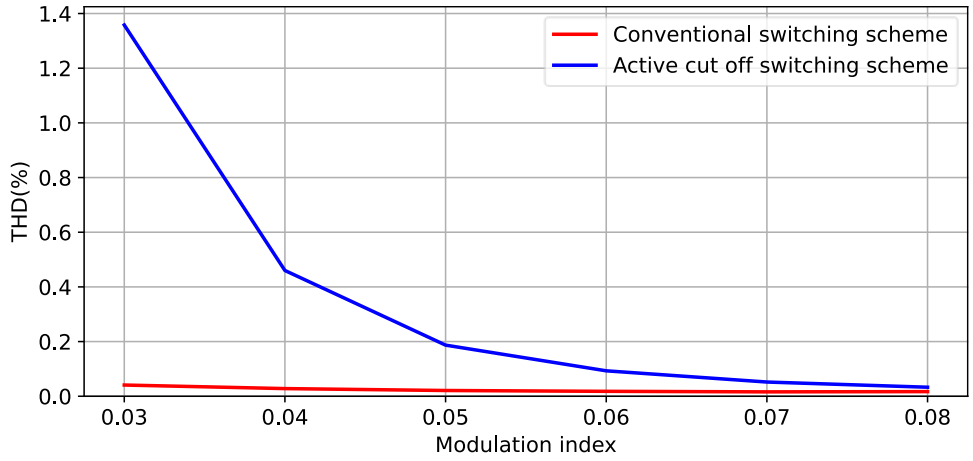


Figure 4.15: *Compare THD of load current over modulation index from conventional and active cut-off switching scheme.*

It is necessary to optimize the switching transition time to get lower THD. Additionally, the shorter transition time also helps to faster cut off the LF oscillation. The optimization can be done by increasing the switching speed or rearrange the switching sequence as describing below.

From the examples above, the level-crossing switching pattern includes four transition steps:

- S1: Turn on the complement IGBT.
- S2: Turn off MOSFET.
- S3: Turn on opposite MOSFET.
- S4: Turn off the IGBT.

Each step Sx, turn on or turn off has basically 2 phases: delay phase (Sx.d) and transient phase (Sx.t). During the turn-off transition, the turn off delay time (Sx.d) is defined from 90% V_{gson} to 10% V_{dsmax}, the turn-off transient time (Sx.t) is from 10% V_{dsmax} to 5% I_{dsmax} like in the Figure 4.16. During the turn-on transition, the turn on delay time (Sx.d) is defined from 10% V_{gson} to 5% I_{dsmax}, the turn-on transient time (Sx.t) is from 5% I_{dsmax} to 10% V_{dsmax} like in the Figure 4.17.

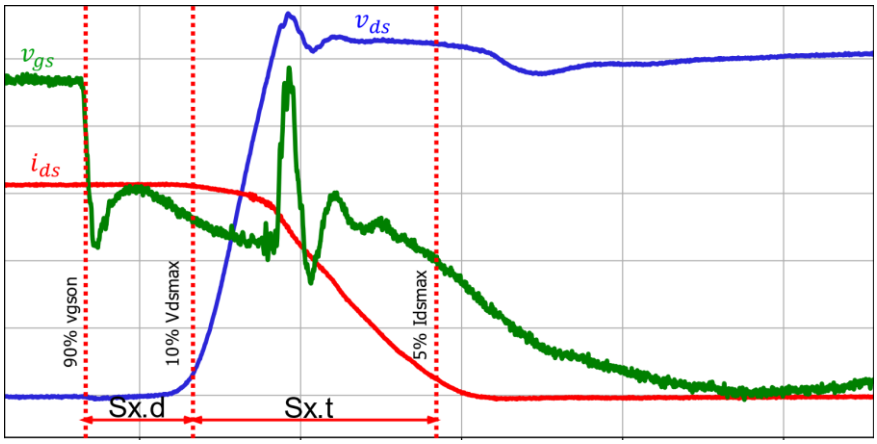


Figure 4.16: *Turn-off's delay phase (Sx.d): from 90% V_{gson} to 10% of the maximum of the operating voltage and the turn-off's transition phase (Sx.t): from 10% of the maximum of the operating voltage to 5% of the maximum of the operating current.*

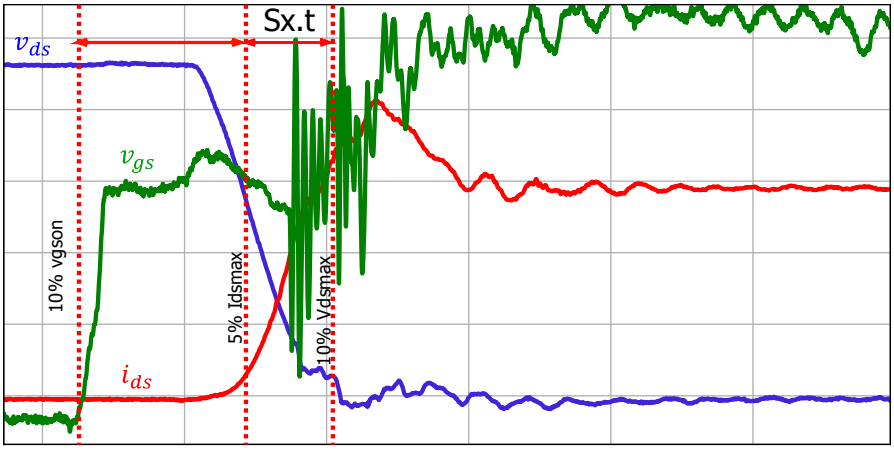


Figure 4.17: *Turn-on's delay phase (Sx.d): from the 10% V_{gson} to 10% of the maximum of the operating current and the turn-on's transition phase (Sx.t): from 5% of the maximum of the operating current to 10 % of the maximum of the operating voltage.*

The Figure 4.18 shows a non-optimal switching schedule of a level-crossing transition. In this schedule, each transition step needs to be completely finished before starting the new one. The trigger time of each step follows the sequence in the Table 4.6. As it can be seen that the oscillation is triggered at the step 2, but until the end of step 4, it is cut off. The calculation of the non-optimal trigger times can be seen in the Table 4.6.

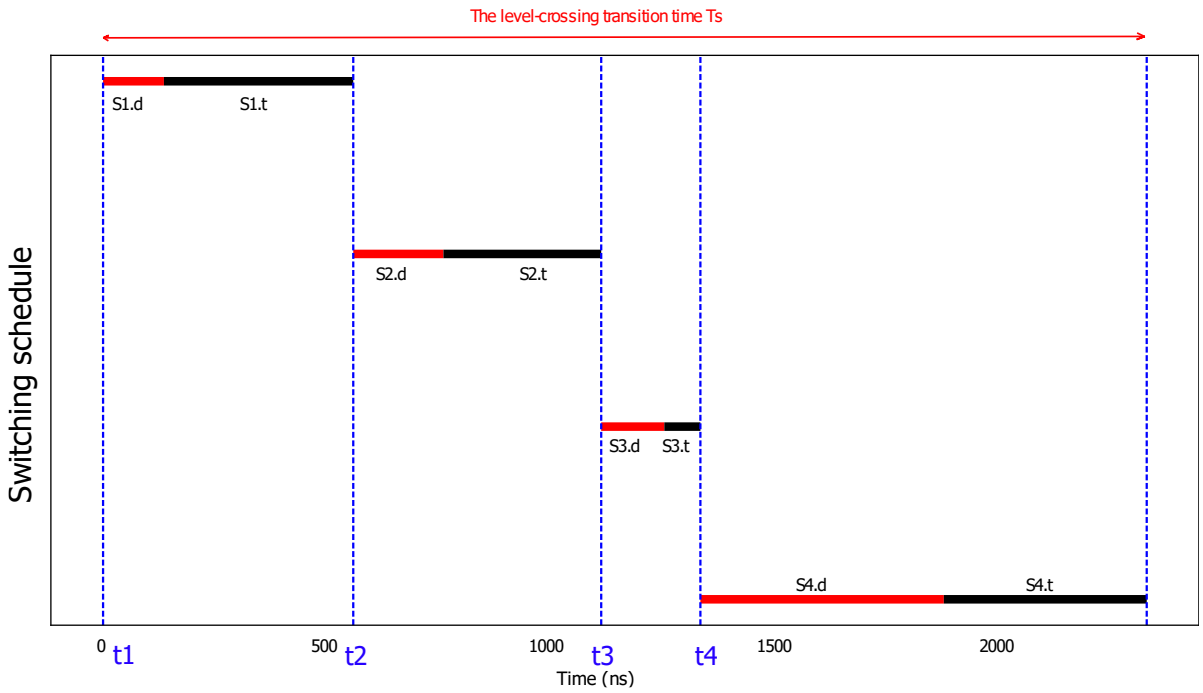


Figure 4.18: *Non-optimal switching schedule of the level-crossing transition. The red line is the delay phase (Sx.d) and the black line is the transient phase (Sx.t).* t_1, t_2, t_3, t_4 *are the trigger events.*

Table 4.6: *Non-optimal trigger times calculation.*

Trigger times	Calculation	Events
t_1	$t_1 = 0$	Turn on IGBT(S1)
t_2	$t_2 = t_1 + S1.d + S1.t$	Turn off MOSFET(S2)
t_3	$t_3 = t_2 + S2.d + S2.t$	Turn on MOSFET(S3)
t_4	$t_4 = t_3 + S3.d + S3.t$	Turn off IGBT(S4)

The total transition time T_s can be calculated as:

$$T_s = S1.d + S1.t + S2.d + S2.t + S3.d + S3.t + S4.d + S4.t \quad (4.5)$$

4.6.1 Level-crossing transition time optimization.

It is possible to shorten the level-crossing transition time by rearranging the switching sequences. The arrangement begins backward from the last step back to the first step like in the Figure 4.19. Because the step S1, S4 are switched at no load current, the transient phase is very short and can be ignored. The S3.t should be finished before the end of S4.d. Similarly, The S2.t should be finished before the end of S3.d. Because S1 has no transient phase, it can start at t_1. A dead time period is added at the end of the step which has the transient phase to ensure the load current completely commutate. The trigger times t_1, t_2, t_3 are recalculated as Table 4.7.

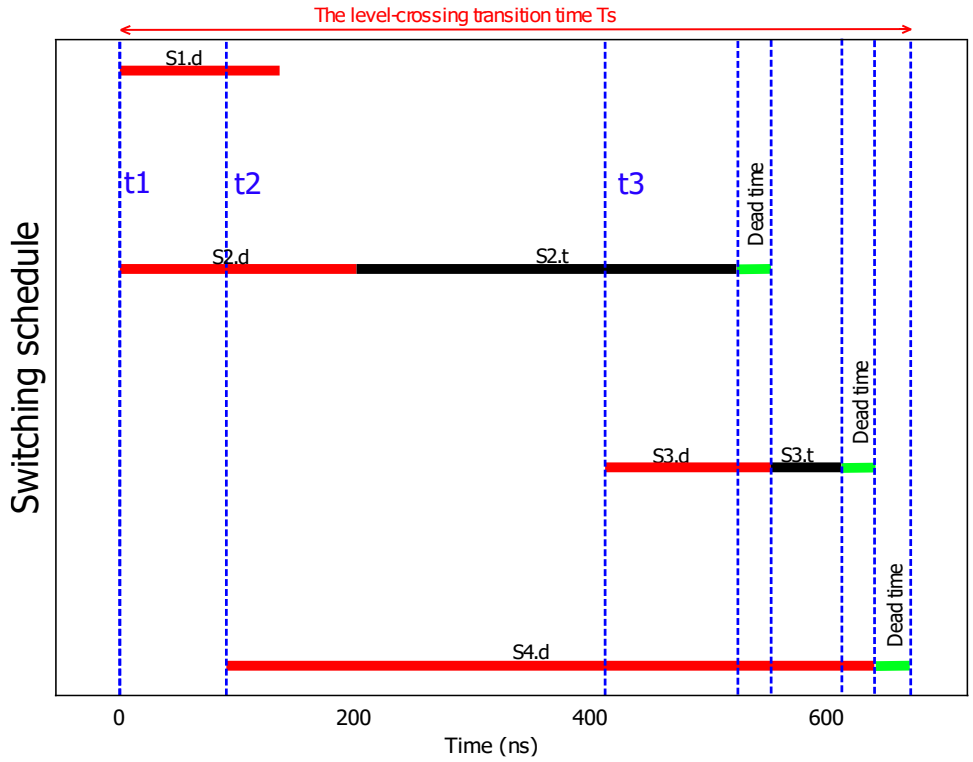


Figure 4.19: *Optimal switching schedule of the level-crossing transition.*

If it is assumed that:

$$\mathrm{S4.d} \leq S2.d + S2.t + S3.t + 2 \cdot Deadtime \quad (4.6)$$

The total transition time T_s is:

$$T_s = S2.d + S2.t + S3.t + 3 \cdot Deadtime \quad (4.7)$$

Comparing to the equation (4.5), the new transition time is significantly shorter.

Table 4.7: *Optimal trigger times calculation.*

Trigger times	Calculation	Events
t_1	$t_1 = 0$	Turn on IGBT(S1) and turn off MOSFET(S2)
t_2	$t_2 = S2.d + S2.t + S3.t + 2 \cdot deadtime - S4.d$	Turn off IGBT(S4)
t_3	$t_3 = S2.d + S2.t + deadtime - S3.d$	Turn on MOSFET(S3)

4.6.2 Zero-crossing transition time optimization

The transition 7, 8, 11, 12, have only two IGBTs changed so there are only two transition steps:

- S1: Turn off the IGBT.
- S2: Turn on the complement IGBT.

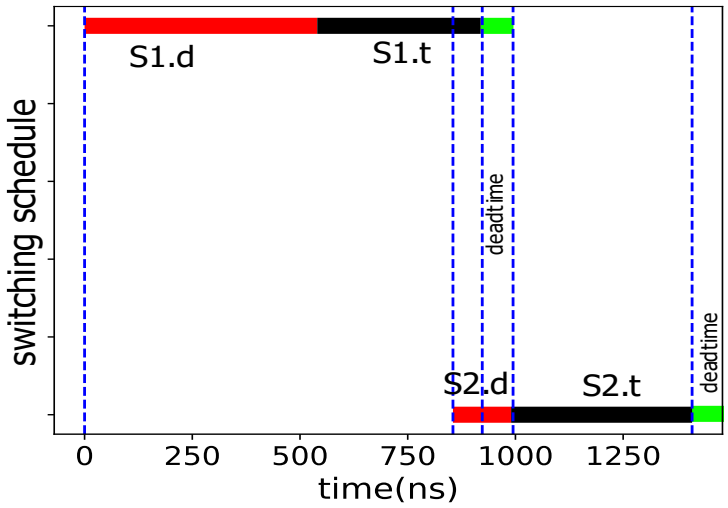


Figure 4.20: *Optimal zero-crossing transition 7, 8, 11, 12 switching schedules. The red lines are the delay phase and the black lines are the transient phase, the green lines are the deadtime.*

The total transition time can be reduced by rearranging the switching schedule similar to the above level-crossing transition which can be seen in the Figure 4.20. The total transition time is:

$$T_s = \ S1.d + S1.t + S2.t + 2 \cdot deadtime \qquad (4.8)$$

It is clearly seen that reducing the turn-off delay time of the IGBT will also reduce the total zero-crossing transition time.

4.6.3 IGBT's turn-off delay time optimization

From (4.6), if the turn-off delay of the IGBT S4.d is too long:

$$S4.d > S2.d \ + \ S2.t \ \ + \ S3.t + 2 \cdot deadtime \qquad (4.9)$$

It will dominate the total level-crossing transition time T_s:

$$T_s = \ S4.d + deadtime \qquad (4.10)$$

Reducing the turn-off delay of the IGBT would result in a shorter transition. It is possible to reduce the turn-off gate resistor to shorten the turn-off delay time. However, this method may lead to the overvoltage due to high speed turn-off. There is a possibility to further decrease the turn-off delay time without the side effect by an additional turn-off capacitor circuit like in the Figure 4.21 which is described in [100].

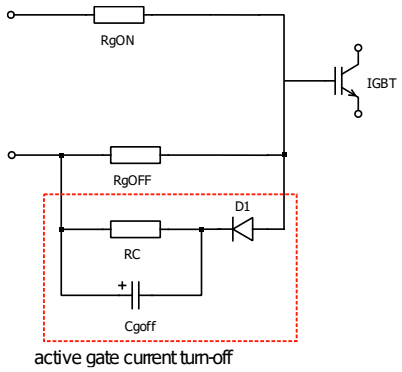


Figure 4.21: *C_{goff} circuit can flash out the IGBT's gate charges faster.*

The principle of the circuit is that: at the beginning of the IGBT's turn-off process, the gate charge is flashed down by C_{goff}. The bigger C_{goff} is, the faster the gate are discharged and

hence the turn-off delay time is shorter. RC resistor is used to discharged C_{goff} during turn-on phase make it ready for the next turn-off process. When the flash-down is finished, the gate current returns to its normal turn-off speed which defined by the R_{goff}.

Figure 4.22 shows the turn-off gate voltage with different value of C_{goff}. The gate flash-down effect can be observed at the first pulse of the gate voltage. With C_{goff} = 100nF, the turn-off delay time can be reduced up to 33% compare to the case without using C_{goff}. The result can be found in the Table 4.8.

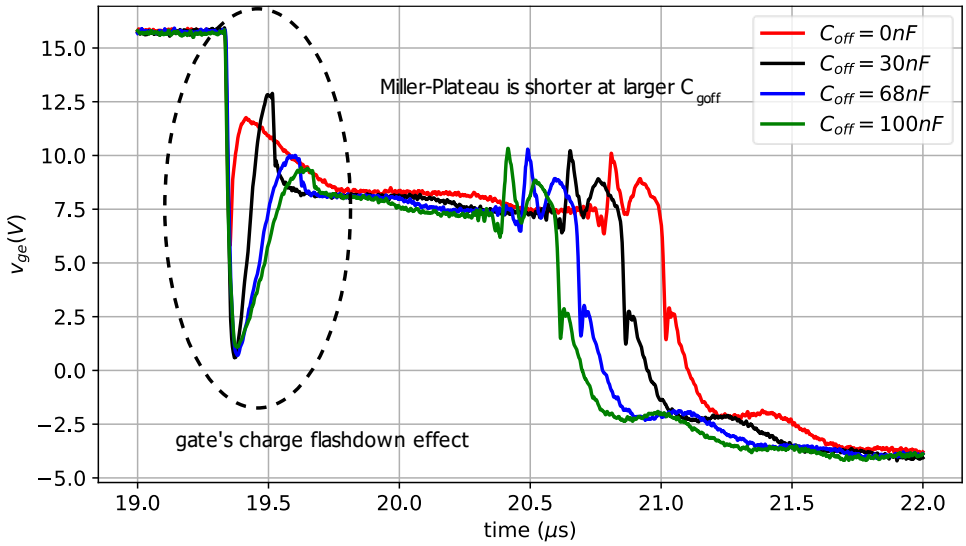


Figure 4.22: *Turn-off gate voltage with different C_{goff} value. The higher C_{goff} is the shorter Miller-Plateau becomes.*

Table 4.8: *Turn-off delay time with different C_{goff} values.*

C_{goff} (nF)	Turn-off delay time (ns)
100	756
68	835
30	1000
0	1142

Figure 4.23 illustrates that the optimized active cut-off switching scheme has notably reduced the minimum turn-on time compared to the non-optimized active cut-off scheme. This

reduction contributes to a significant decrease in current distortion, as visually depicted in Figure 4.25. The result of the transient time optimization can be seen in the Figure 4.24 which reduces significantly the THD of the load current.

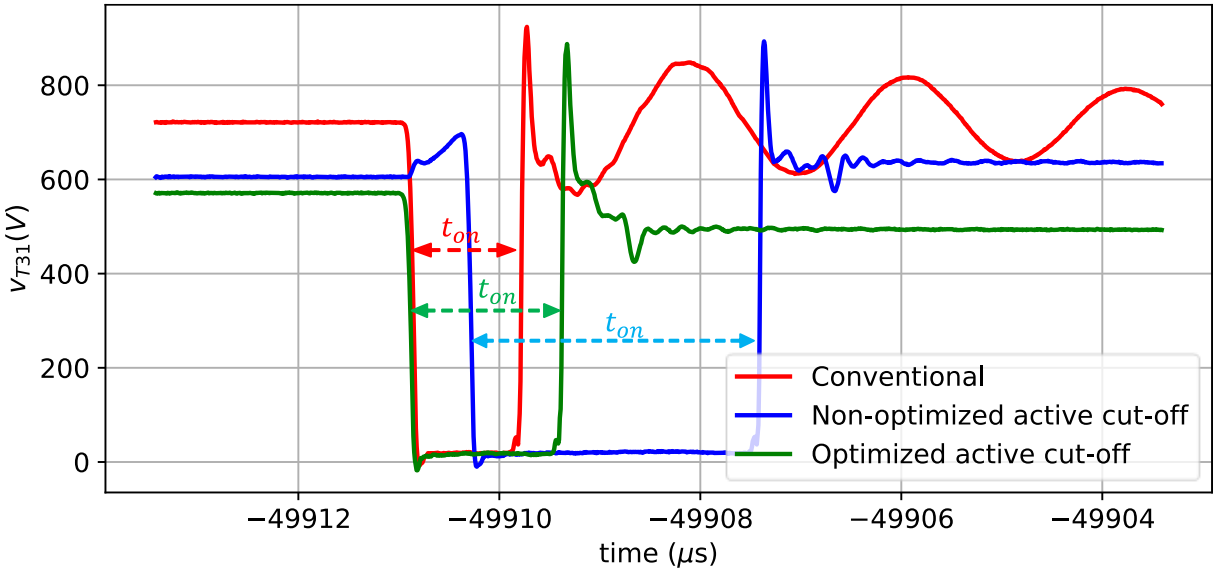


Figure 4.23: *Compare the smallest t_{on} time at the peak of the load current between the conventional switching scheme (dashed red arrow), the non-optimized active cut-off (dashed blue arrow) and the optimized active cut-off (dashed green arrow). The voltage across T31 during the P, ZP transitions at IL = 450A.*

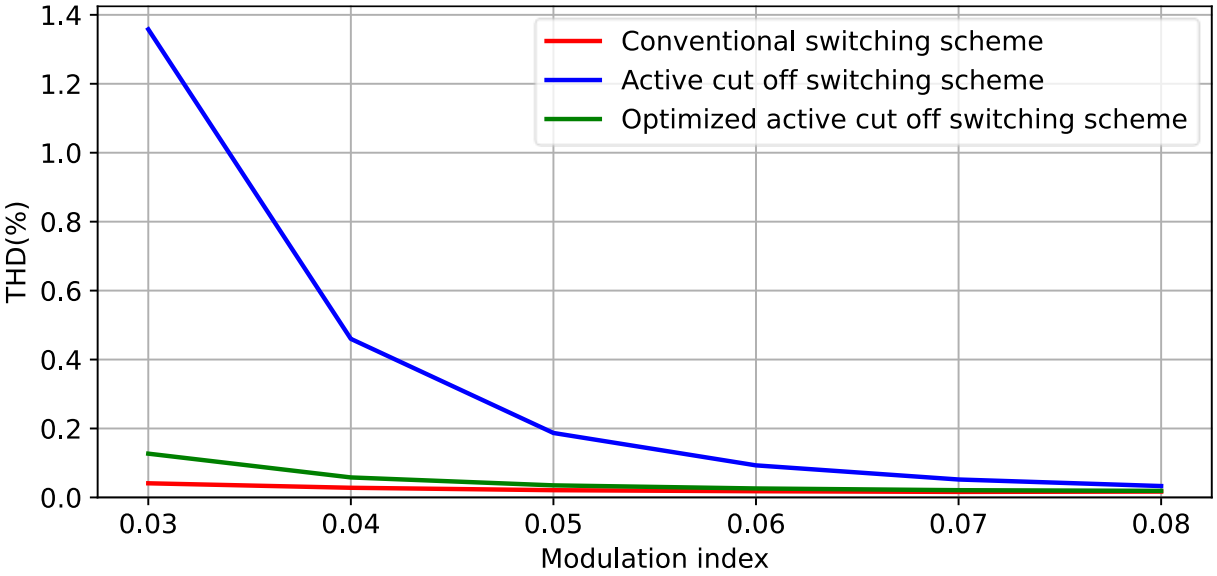


Figure 4.24: *Level-crossing transition time optimization leads to lower load current THD at low modulation index.*

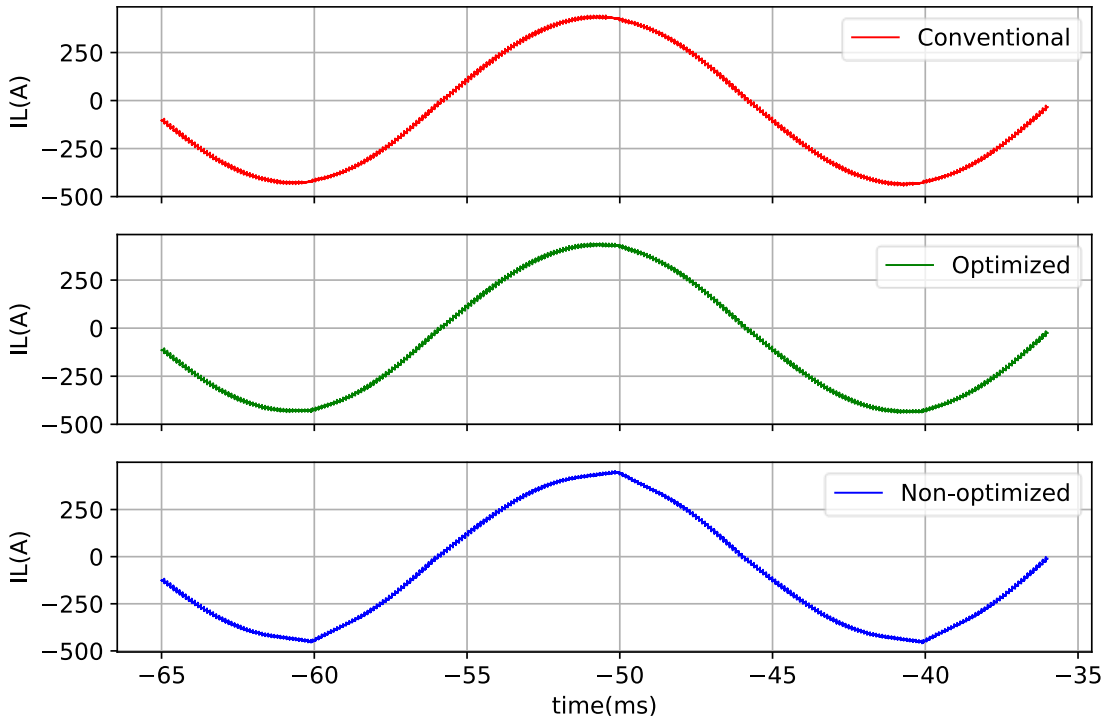


Figure 4.25: *Load current waveform with different switching schemes: Conventional (red line), optimized active cut-off (green line) and non-optimized active cut-off (blue line).*

In summary, the low-frequency oscillation can be effectively eliminated by deactivating one of the IGBTs that isn't handling the load current. Since the presence of load current is always defined when one of the SiC MOSFETs is active, identifying the specific IGBT to deactivate is straightforward regardless of the load current's direction. The only period when the load current's position is uncertain is during the dead time when both SiC MOSFETs are inactive. To ensure the switching process remains unaffected by the load current's direction during this dead time, both IGBTs are activated.

One drawback of the active cut-off switching scheme is its long transition time, leading to current distortion at extremely low or high modulation indices. This transition time can be minimized by reorganizing the switching sequence and decreasing the turn-off delay time of the IGBT using C_{goff}. Additionally, due to the imbalance between the charging and discharging processes of the decoupling capacitor during the cut-off scheme, the voltage of the decoupling capacitor drifts from $V_{DC}/2$. This effect results in switching losses on the IGBTs and complicates the estimation process of the IGBT's switching losses.

5. Turn-on Losses Optimization and Overvoltage Protection

The intrinsic body diode of a SiC MOSFET has distinctive characteristics that set it apart from silicon-based free-wheeling diodes. These characteristics vary mainly depending on two parameters: the MOSFET's junction temperature and load current.

At low temperatures and low currents, the total reverse-recovery charge (Q_{rr}) is primarily dominated by the output capacitor charge (Q_{oss}) and the amount of bipolar charge (Q_{bip}) is very low. However, as temperature and current increase, more bipolar charges are accumulated within the body diode, eventually becoming the predominant component of the total reverse-recovery charge. This increasing in bipolar charge contributes to a snappy reverse-recovery process, resulting in higher overvoltage, pronounced ringing, and greater reverse-recovery losses [104, 29, 30]. Therefore, the turn-on speed is limited to protect the device from destruction. The price for safeguard the device from this snappy behavior is higher turn-on losses.

P. Hofstetter's work in [31] highlights that the parasitic turn-on (PTO) effect can result in a less abrupt reverse-recovery behavior of the body diode by increasing the turn-off gate voltage. When the overvoltage and ringing are reduced, it becomes feasible to increase the turn-on speed, thereby achieving a reduction in overall turn-on and reverse-recovery losses. Several questions remain open regarding the optimization of this method. For instance, there is a need to determine the optimal turn-off gate voltage and determining the appropriate turn-on gate resistance. Additionally, it is important to explore how this method performs when the threshold voltage of the device changes, particularly under varying operating temperatures or as a result of aging effects.

In this chapter, these topics are extensively investigated, aiming to provide a deeper understanding of the method's principle and how to effectively implement it under various operating conditions. Furthermore, the author introduces a novel concept by demonstrating how to employ active clamping for the purpose of protecting the device, not only from turn-off overvoltage but also from reverse-recovery overvoltage. This approach ultimately enhances the reliability and performance of the device.

5.1 Parasitic turn-on in a half-bridge SiC MOSFET module

The double pulse test setup is shown in Figure 5.1 with more detail of T31 parasitic elements. These capacitors C_{gd}, C_{gs}, C_{ds} are MOSFET T31's internal capacitors, L_{sin} is the internal stray inductance of the source terminal of T31, L_{gin} and R_{gin} are T31's internal gate inductance and resistance. L_p is stray inductance between DC link voltage source and the MOSFET modules. According to [112], there is also a magnetic coupling M_g between the gate network and the power circuit in the SiC MOSFET module. The voltage induced by the magnetic coupling can be added or subtracted to the gate voltage depends on the internal layout of the module and it is different from manufacturers to manufacturers.

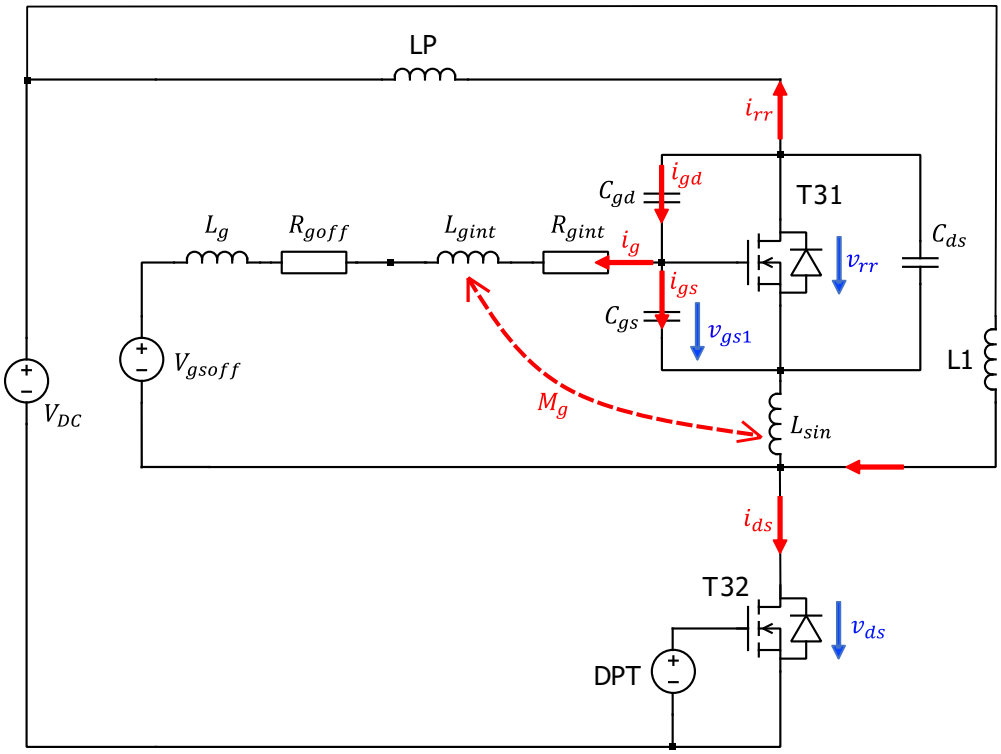


Figure 5.1: *SiC MOSFET half-bridge double pule test set-up with detail T31 parasitic elements and magnetic coupling Mg between T31's gate circuit network and* $\frac{di_{ds}}{dt}$ *of T32.*

The double pulse test is applied on the lower MOSFET T32, the upper MOSFET T31 is off at adjustable gate voltage V_{gsoff} . The voltage and current across T31 (v_{rr}, i_{rr}) were measured to calculate the reverse-recovery energy E_{rr}. The voltage and current across T32 (v_{ds}, i_{ds}) were measured to calculate turn-on energy E_{on} of T32. The parasitic turn-on may happen at T31 during the turn-on of T32. When the load current IL is taken over by T32, the

voltage across T31 is raising at speed $\frac{dv_{rr}}{dt}$. The displacement current i_{gd} of C_{gd} then flows through the gate i_g and also C_{gs}, pulling up T31's gate voltage. T31's gate voltage at this time can be modeled by the equation:

$$V_{gsoff} = -(R_{goff} + R_{gin})i_g - (L_g + L_{gin})\frac{di_g}{dt} + v_{gs1} - (M_g + L_{sin})\frac{di_{rr}}{dt} \quad (5.1)$$

$$i_{gd} = i_g + i_{gs} \leftrightarrow i_g = C_{gd}\frac{dv_{rr}}{dt} - (C_{gs} + C_{gd})\frac{dv_{gs1}}{dt} \quad (5.2)$$
$$= C_{gd}\frac{dv_{rr}}{dt} - C_{iss}\frac{dv_{gs1}}{dt}$$

In case of having low gate inductance and low internal gate resistance, equation (5.1) can be approximated:

$$v_{gs1}(t) \approx \underbrace{V_{gsoff}}_{static} + \underbrace{R_{goff}\,C_{gd}\cdot\frac{dv_{rr}}{dt}}_{voltage\ dynamic} + \underbrace{\left(M_g + L_{sin}\right)\cdot\frac{di_{rr}}{dt}}_{current\ dynamic} \quad (5.3)$$

Equation (5.3) is a combination of 3 components: V_{gsoff} is the static component, the voltage dynamic component: $R_{goff}\,C_{gd}\cdot\frac{dv_{rr}}{dt}$ and the current dynamic component: $\left(M_g + L_{sin}\right)\cdot\frac{di_r}{dt}$. During the reverse-recovery of the body diode, it is possible to divide the process into two main regions like the Figure 5.2:

- Region A: This occurs before the reverse-recovery current peak, in this region, $\frac{dv_{rr}}{dt} = 0$ and $\frac{di_{rr}}{dt} < 0$. If $M_g + L_{sin} > 0$, the gate voltage is pulled down by $\frac{di_{rr}}{dt}$.
- Region B: This takes place after the reverse-recovery current peak, in this region, $\frac{dv_{rr}}{dt} > 0$ and $\frac{di_{rr}}{dt} > 0$. If $M_g + L_{sin} > 0$, the gate voltage is pulled up by both $\frac{di_{rr}}{dt}$, $\frac{dv_{rr}}{dt}$. Depend on the static voltage V_{gsoff}, the total gate voltage of T31 in this region can exceed the threshold voltage ($v_{gs1} > v_{th}$), leading to parasitic turn-on and a short-circuit current runs through both T31 and T32. In Figure 5.2, when the V_{gsoff} = -3V, the upper gate voltage v_{gs1} is lifted above the threshold voltage during $\frac{dv_{rr}}{dt} > 0$, the parasitic turn-on happens.

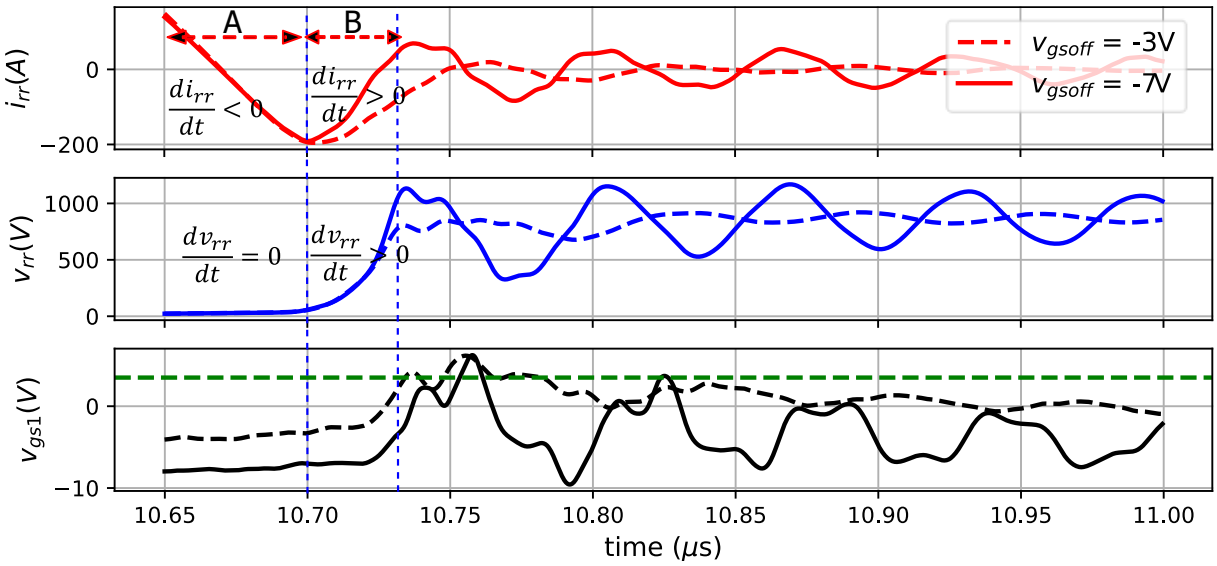


Figure 5.2: *The upper gate voltage (v_{gs1}) at different di/dt and du/dt phase during the turn-on of T32 at turn-off gate voltage V_{gsoff} = -3V (dashed lines) and V_{gsoff} = -7V (solid lines) compare to the threshold voltage (dashed green line). Module FF3MR12KM1P with Kelvin terminal, V_{DC} = 900V, IL =600A, T_j =150°C, V_{th} = 3.15V.*

5.2 Reverse-recovery of SiC MOSFET's body diode

The turn-on process of T32 are described in the Figure 5.3.

t_0: The input capacitor of T32 starts being charged, v_{gs2} is rising

t_1: v_{gs2} reaches the threshold voltage $v_{gs2} = V_{th}$

t_2: The reverse current $i_{rr} = 0$

t_3: The reverse current reaches its peak I_{rrmax}

t_4: The reverse current return to zero $i_{rr} = 0$

The reverse-recovery charge, denoted as Q_{rr}, is determined by integrating the reversed current $i_{rr}(t)$ over the time period from t_2 to t_4. It comprises two main components: the bipolar charge Q_{bip}, originating from the electron-hole plasma remaining in the drift region after turning off the body diode [103]. This charge is highly sensitive to both junction temperature and load current [96, 102]. Greater forward load currents push more plasma into the drift region, and at

higher temperatures, carrier lifetimes are extended, resulting in an increase in bipolar charge. The capacitive charge Q_{oss}, associated with the output capacitance C_{oss} [104]. Due to the thin drift layer in the 1.2kV SiC MOSFET, capacitive charge dominates at room temperature [104]. Unlike bipolar charge, capacitive charge is mostly unaffected by load current and junction temperature, its primary dependency is on the device's voltage. The reverse current, $i_{rr}(t)$, during reverse-recovery can thus be modeled as the sum of the output capacitor current, $i_{coss}(t)$, and the bipolar current of the body diode, $i_{bd}\ (t)$, as expressed in equation (5.5).

$$i_{coss}(t) = C_{oss} \cdot \frac{dv_{rr}}{dt} \tag{5.4}$$

$$i_{rr}(t) = i_{coss}(t) + i_{bd}(t) \tag{5.5}$$

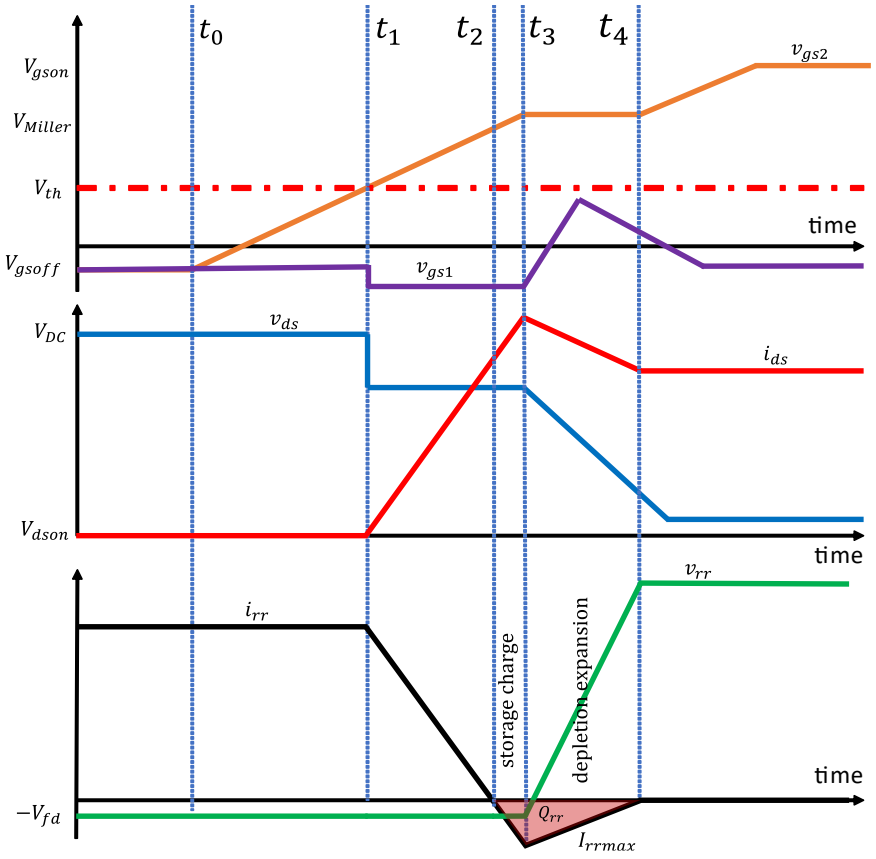


Figure 5.3: *Turn-on process of T32 and the reverse-recovery on T31's body diode.*

Different from the PiN diode in IGBT, the MOSFET's body diode has the channel connected in parallel. The changing of the gate voltage during the reverse-recovery may change the channel's conduction state and hence its reverse-recovery behavior. During the reverse-

recovery, T31's gate voltage is sensitive to both di/dt and du/dt of the process. Assumed that the MOSFET T31 is permanently off at V_{gsoff}, according to the equation (5.3), in the period $t_1 < t < t_3, \frac{dv_{rr}}{dt} = 0, \frac{di_{rr}}{dt} < 0$, the gate-source terminal voltage of T31 v_{gs1} is dropped to:

$$v_{gs1} = v_{gsoff} + \left(M_g + L_{sin}\right) \cdot \frac{di_{rr}}{dt} \quad (5.6)$$

And during $t_3 < t < t_4, \frac{dv_{rr}}{dt} > 0, \frac{di_{rr}}{dt} > 0$, T31's gate voltage is pulled up:

$$v_{gs1} = v_{gsoff} + \left(M_g + L_{sin}\right) \cdot \frac{di_{rr}}{dt} + R_{goff}\, C_{gd} \frac{dv_{rr}}{dt} \quad (5.7)$$

After t_4, the gate of T31 is discharged through R_{gsoff}, its gate voltage returns back to V_{gsoff}.

5.3 Reverse-recovery under parasitic turn-on effect

During the depletion phase, the voltage of the body diode rising at the rate of $\frac{dv_{rr}}{dt}$. If the voltage slope is high enough, the gate voltage of T31 can be lifted above the threshold voltage which turns on the channel temporarily and lets the short-circuit current runs through it. The effect increases the reverse-recovery losses but it also has some positive effects:

- The channel is on which clamps the voltage slope $\frac{dv_{rr}}{dt}$ to zero. Reducing the $\frac{dv_{rr}}{dt}$ benefits the EMI performance.
- The cross-current through the channel $i_{cn}(t)$is added to the sum of the diode current $i_{bd}(t)$ and capacitor current $i_{coss}(t)$. The total current slope is reduced, the effect makes the reverse-recovery softer.
- When the reverse-recovery less abrupt, the oscillation and the overvoltage during the reverse-recovery are also reduced.

The reverse-recovery current under the parasitic turn-on effect can be modeled with three parallel components like in the Figure 5.4. The reverse-recovery current $i_{rr}(t)$ is the sum of the output capacitor's current $i_{coss}(t)$, the channel current $i_{cn}(t)$ and the body diode's current $i_{bd}(t)$.

$$i_{rr}(t) = i_{cn} + i_{coss} + i_{bd} \quad (5.8)$$

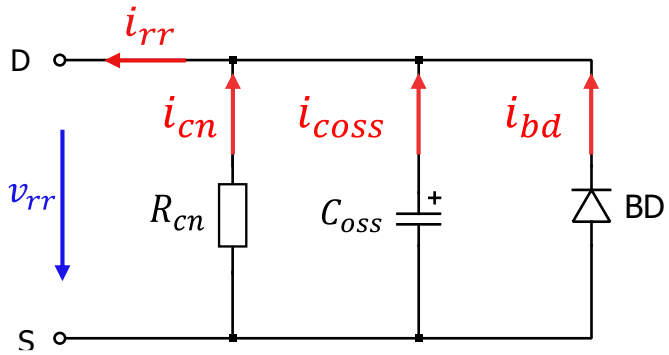


Figure 5.4: *Equivalent circuit of the MOSFET during its body diode's reverse-recovery under parasitic turn-on.*

The effect of parasitic turn-on on reverse-recovery behavior was investigated through double pulse tests. These tests were carried out with a fixed V_{DC} of 900V, an IL of 600A, R_{gon} of 5.6Ω, R_{goff} of 5.1 Ω, and a junction temperature (T_j) of 150°C. The MOSFET T31 was turned off at different gate-source voltages (V_{gsoff}) of [-7V, -3V, -2V, -1V].

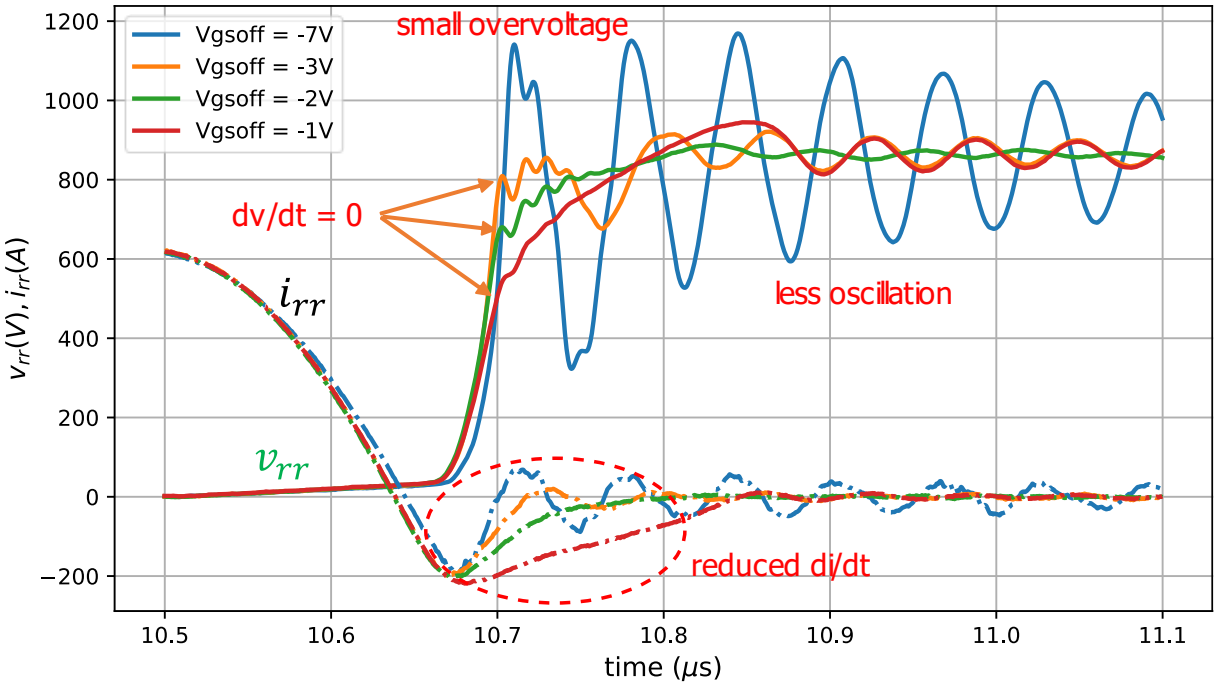


Figure 5.5: *Three positive effects of parasitic turn-on effect during the depletion phase of the reverse-recovery. V_{DC} = 900V, IL= 600A, R_{gon} = 5.6 Ω, R_{goff} =5.1 Ω, T_j = 150°C, V_{gsoff} = [-7V, -3V, -2V, -1V].*

The experimental results, depicted in Figure 5.5, reveal that when V_{gsoff} increases, the reverse-recovery current slope di_{rr}/dt becomes softer. This softening effect leads to reduced oscillations, lower overvoltage, and a decrease in dv_{rr}/dt.

5.4 Reverse-recovery overvoltage protection

Active clamping is well-known for protecting SiC MOSFET from the turn-off overvoltage. In the half-bridge module, the diode chains are always implemented for both upper and lower MOSFET. In case of turning on the lower MOSFET, the reverse-recovery happens on the upper MOSFET, if the reverse-recovery voltage on the upper MOSFET is more than the breakdown voltage of the diode chain, its gate voltage is pulled up. Because SiC MOSFET is off at quite high gate voltage (usually -5V) compare to IGBT (usually -15V), which makes the SiC MOSFET more sensitive to parasitic turn-on. Together with parasitic turn-on and the effect of the active clamping circuit, the induced gate voltage of the upper MOSFET in this case can be large enough to turn it on again. The behaviors of the upper MOSFET and its body diode in this scenario are explained in this section. From the understanding of the mechanism, the author suggests the principle to actually use the active clamping for the reverse-recovery overvoltage protection. This means, the active clamping can protect SiC MOSFET half-bridge in both turn-on, turn-off transients.

5.4.1 Reverse-recovery overvoltage and oscillation modeling

Figure 5.6 depicts the turn-on of T32 with gate resistance R_{gon}, T31 is off with gate resistance R_{goff} at V_{gsoff}. The voltage and current through T31's body diode are v_{rr}, i_{rr}, the voltage and current through the lower MOSFET T32 are v_{ds}, i_{ds}. L_2, R_2 are the commutation loop's inductance and resistance. C_{oss} is the output capacitor of the upper MOSFET. Figure 5.7 shows regular reverse-recovery waveforms of the voltage and current across the upper MOSFET. The time t_1, t_2, t_3, t_4 are marked at the corresponding events:

t_1: The free-wheeling current starts dropping and the lower MOSFET voltage v_{ds} falls due to the loop stray inductance L_2. v_{ds} can be dropped faster at higher di_{ds}/dt or larger L_2.

t_2: marks the time when the reverse current reaches its peak value.

t_3: is when the reverse-recovery current returns to zero.

t_4: is when the lower MOSFET is completely turned on.

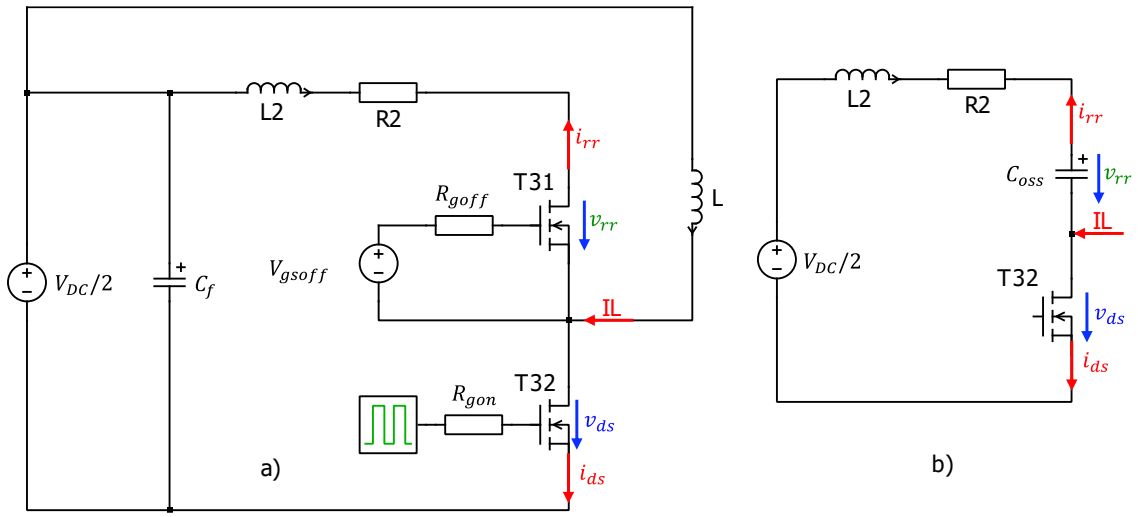


Figure 5.6: *a) Equivalent circuit of 2SiC Hybrid ANPC during the reverse-recovery of T31's body diode, b) Small signal circuit during the turn-on of T32.*

The reverse-recovery's overvoltage was well known because of the reverse-recovery current slope between t_2 and t_3 and the commutation loop's stray inductance [111, 105]. For the time after t_3, when the switching oscillation starts, the overvoltage is more complex which may include also the oscillation's amplitude, which is usually underestimated and ignored. Hence, it is more important to modelling the body diode's voltage in this period. Choose $t = 0$ at t_3, when $i_{rr} = 0$, apply the current Kirchhoff 's law for the circuit in Figure 5.6b after t_3.

$$\frac{V_{DC}}{2} = -L_2 \cdot \frac{di_{rr}(t)}{dt} - R_2 \cdot i_{rr}(t) + v_{rr}(t) + v_{ds}(t) \quad (5.9)$$

When $t_3 < t < t_4$, assumed that $v_{ds}(t)$ reduces at a constant rate b (V/s) to zero. $v_{ds}(t)$ can be modeled:

$$v_{ds}(t) = \begin{cases} v_{ds0} - bt & when \;\; t_3 < t < t_4 \\ 0 & when \; t > t4 \end{cases} \quad (5.10)$$

With v_{ds0} is T32's voltage at t_3. The voltage slope b is calculated by:

$$b = \frac{v_{ds0}}{t_4 - t_3} \quad (5.11)$$

Replace (5.10) to (5.9), when $t_3 < t < t_4$,

$$\frac{V_{DC}}{2} - v_{ds0} + bt = -L_2 \cdot \frac{di_{rr}(t)}{dt} - R_2 \cdot i_{rr}(t) + v_{rr}(t) \quad (5.12)$$

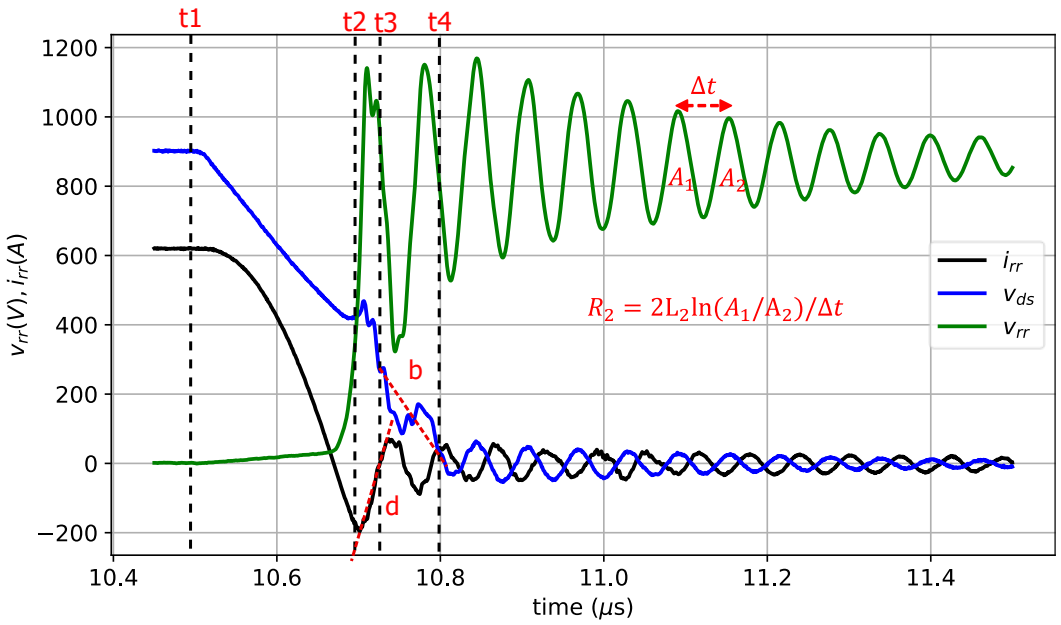


Figure 5.7: *Regular reverse-recovery waveform and the commutation circuit's resistance R2 and inductance L_2 extraction from the measured waveform.*

Assumed that there is no parasitic turn-on and the body diode current is zero during the time $t_3 < t < t_4$, the reverse-recovery current is equal to the capacitor current.

$$i_{rr} = i_{coss} = I_L - i_{ds} \quad (5.13)$$

$$v_{rr}(t) = \frac{-1}{C_{oss}} \cdot \int i_{rr}(t) \cdot dt \quad (5.14)$$

Replace (5.14) to (5.12)

$$\frac{-V_{DC}}{2} + v_{ds0} - bt = L_2 \cdot \frac{di_{rr}(t)}{dt} + R_2 \cdot i_{rr}(t) + \frac{1}{C_{oss}} \int i_{rr}(t)dt \quad (5.15)$$

Differentiate 2 sides of (5.15)

$$L_2 i''_{rr} + R_2 i'_{rr} + \frac{1}{C_{oss}} i_{rr} = -b \quad (5.16)$$

The solution of this type of differential equation has two parts: the complementary function and the particular integral. The overall solution is the sum of those two parts. The particular integral is linear so the solution is [54]:

$$i_{rr} = k = const \tag{5.17}$$

Replace (5.17) to the original equation (5.16) with $i_{rr}'' = k'' = 0, i_{rr}' = k' = 0$

$$L_2 k'' + R_2 k' + \frac{1}{C_{oss}} k = -b \tag{5.18}$$

$$i_{rr} = k = -bC_{oss} \tag{5.19}$$

The complementary part is the ordinary differential equation:

$$L_2 i_{rr}'' + R_2 i_{rr}' + \frac{1}{C_{oss}} i_{rr} = 0 \tag{5.20}$$

The characteristic equation of Equation (5.20) is

$$L_2 r^2 + R_2 r + \frac{1}{C_{oss}} = 0 \tag{5.21}$$

The roots of this differential equation:

$$r_1 = \frac{-R_2 - \sqrt{R_2^2 - 4L_2/C_{oss}}}{2L_2} \tag{5.22}$$

$$r_2 = \frac{-R_2 + \sqrt{R_2^2 - 4L_2/C_{oss}}}{2L_2} \tag{5.23}$$

If it is an underdamped case where $R_2 < \sqrt{4L_2/C_{oss}}$, the solution to the ordinary equation (5.21) is

$$i_{rr}(t) = A \cdot e^{-\alpha t} \cdot \cos(\omega t - \theta) \tag{5.24}$$

Where the attenuation factor and the oscillation frequency are:

$$\alpha = \frac{R_2}{2L_2} \tag{5.25}$$

$$\omega = \sqrt{\frac{1}{L_2 C_{oss}} - \left(\frac{R_2}{2L_2}\right)^2} \approx 1/\sqrt{L_2 C_{oss}} \tag{5.26}$$

The overall solution will be the sum of (5.19) and (5.24)

$$i_{rr}(t) = A \cdot e^{-\alpha t} \cdot \cos(\omega t - \theta) - bC_{oss} \tag{5.27}$$

$$\frac{di_{rr}}{dt} = -\alpha A \cdot e^{-\alpha t} \cdot \cos(\omega t - \theta) - \omega A \cdot e^{-\alpha t} \cdot \sin(\omega t - \theta) \tag{5.28}$$

Apply the initial condition at $t = 0$, $i_{rr}(0) = 0$:

$$c_1 = A \cdot \cos(\theta) = bC_{oss} \tag{5.29}$$

Assumed that the reverse-recovery slope is equal to $\frac{di_{rr}}{dt} = d = const$, at t = 0:

$$d = \omega A \cdot \sin(\theta) - \alpha A \cdot \cos(\theta) \tag{5.30}$$

Replace (5.29) to (5.30)

$$c_2 = A \cdot \sin(\theta) = \frac{d + \alpha b C_{oss}}{\omega} \tag{5.31}$$

From (5.29), (5.31),

$$A = \sqrt{c_1^2 + c_2^2} \tag{5.32}$$

$$\theta = \arctan\left(\frac{c_2}{c_1}\right) \tag{5.33}$$

Replace (5.27), (5.28) to (5.12)

$$v_{rr}(t) = \frac{V_{DC}}{2} - v_{ds0} + bt \tag{5.34}$$

$$+ L_2 \cdot (-\alpha A \cdot e^{-\alpha t} \cdot \cos(\omega t - \theta) - \omega A \cdot e^{-\alpha t} \cdot \sin(\omega t - \theta))$$

$$+ R_2 \cdot (A \cdot e^{-\alpha t} \cdot \cos(\omega t - \theta) - bC_{oss})$$

$$v_{rr}(t) = \frac{V_{DC}}{2} - v_{ds0} - R_2 bC_{oss} + bt \tag{5.35}$$

$$+ Ae^{-\alpha t} \cdot \left(\frac{R_2}{2} \cdot \cos(\omega t - \theta) - \omega L_2 \cdot \sin(\omega t - \theta)\right)$$

$$v_{rr}(t) = \frac{V_{DC}}{2} - v_{ds0} - bR_2 C_{oss} + bt + Ae^{-\alpha t} \cdot \sqrt{L_2/C_{oss}} \cdot \sin(\omega t - \theta + \varphi) \tag{5.36}$$

With

$$\varphi = -\arctan\left(\frac{\alpha}{\omega}\right) \tag{5.37}$$

To qualify the analytical model in (5.36), double pulse tests were conducted using the 62mm SiC MOSFET module FF3MR12KM1P under specific conditions. The tests were carried out at 900VDC and 450A, with a junction temperature of 150°C. To simplify calculations, a standard 2-level busbar configuration was utilized without a decoupling capacitor. The commutation loop inductance was determined by measuring the voltage drop during the second turn-on pulse, resulting in a value of 44.5nH.

Three distinct switching cases were measured to compare with the model's calculations. These cases likely represent different voltage slope *b* and current slope *d*. By comparing the measured results with the calculations derived from the model, the accuracy and reliability of the model can be assessed and validated.

Case 1: R_{gon} = 4.7 **Ω**, R_{goff} = 2.2 **Ω**, V_{gsoff} = -7V, V_{gson} = 15V

Case 2: R_{gon} = 4.7 **Ω**, R_{goff} = 2.2 **Ω**, V_{gsoff} = -2V, V_{gson} = 15V

Case 3: R_{gon} = 2.2 **Ω**, R_{goff} = 2.2 **Ω**, V_{gsoff} = -2V, V_{gson} = 15V

The output capacitor of the SiC MOSFET module operating at 900V is specified as 1.86 nF according to the manufacturer's datasheet [109]. The circuit resistance is determined by analyzing the degraded oscillation amplitudes depicted in Figure 5.7. Where A_1, A_2 are the oscillation amplitudes which are measured at 2 different time points which have the time different Δt, the attenuation factor $\alpha = R_2/2L_2$.

$$\frac{A_1}{A_2} = e^{-\alpha(t_1 - t_2)} \quad (5.38)$$

$$R_2 = 2L_2 \cdot \frac{\ln\left(\frac{A_1}{A_2}\right)}{\Delta t} \quad (5.39)$$

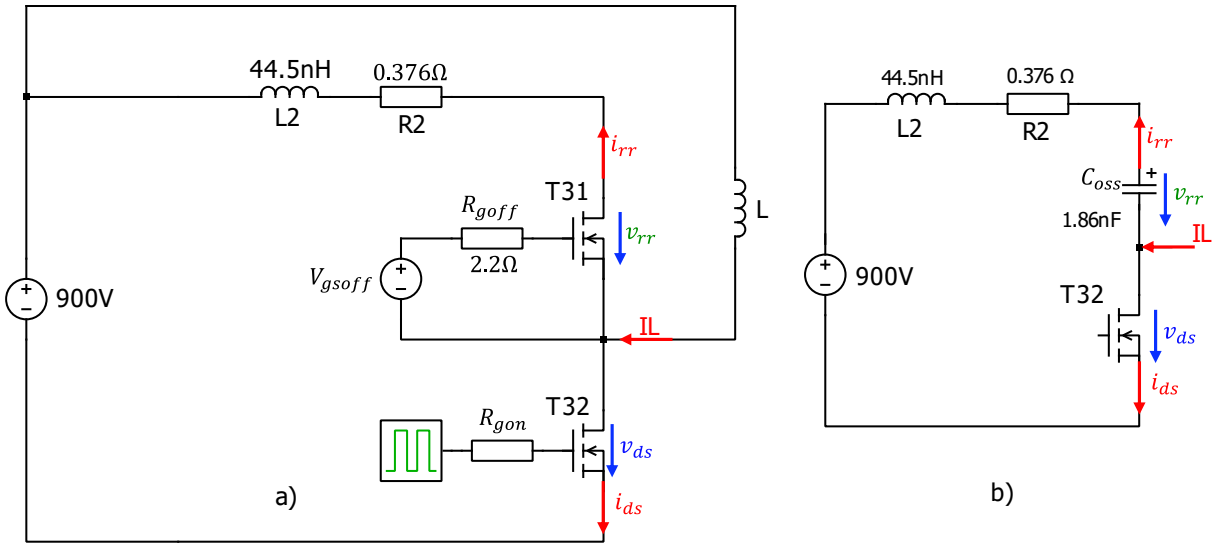


Figure 5.8: *Two-level double pulse test experiment to verify the analytical model proposed in equation* (5.36). *a) The 2-level turn-on double pulse test schematic, b) Equivalent circuit at the reverse-recovery t= t_3.*

The extraction gives the result: $R_2 = 0.376\ \Omega$. The others parameters: v_{ds0}, d, b are independently extracted from the measurements for each case. Because the MOSFET module has the stray inductance at the drain terminal, approximately $L_m = 10nH$ per MOSFET (can be estimated from the increasing of v_{rr} during di/dt phase), the calculated reverse-recovery voltage v_{rr} is lower than the actual measured value at $t = 0$ due to the recovery current slope. To compensate for the error, the measured v_{ds0} should be subtracted the voltage drop across the module's stray inductance $L_m.d$ like in equation (5.40).

$$V_{DC} - v_{ds0} + bt = -L_2 \cdot \frac{di_{rr}(t)}{dt} - R_2 \cdot i_{rr}(t) + \underbrace{v_{rr}(t) - L_m d}_{real\ v_{rr}} \quad (5.40)$$

$$V_{DC} - \underbrace{(v_{ds0} - L_m d)}_{v_{ds0}\ compensated} + bt = -L_2 \cdot \frac{di_{rr}(t)}{dt} - R_2 \cdot i_{rr}(t) + v_{rr}(t) \quad (5.41)$$

The calculated reverse-recovery voltage $v_{rr}(t)$ is compared with the measurement result which can be seen in the Figure 5.9, Figure 5.10, Figure 5.11.

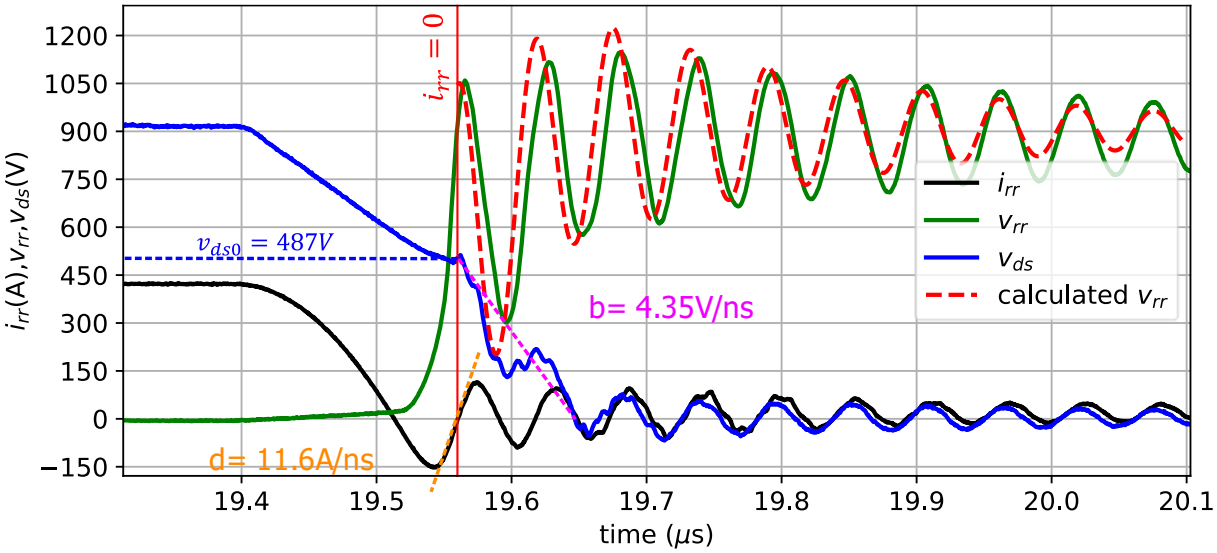


Figure 5.9: *Case 1: R_{gon} = 4.7 Ω, R_{goff} = 2.2 Ω, V_{gsoff} = -7V, V_{gson} = 15V, fitting the calculated model (red dashed line) to the measurement result (green line).*

It can be seen that the model in equation (5.36) of the reverse-recovery voltage is well fit to the measurement results, the different is due to the assumption of the voltage and current slopes are constant. Apart from that, the extracted parameters errors and the measurement errors also contribute to the difference between the calculation and the measurement results.

The equations (5.29), (5.31), (5.32) show that the amplitude of the oscillation strongly depends on the reverse-recovery current slope d and the falling voltage slope b of the lower MOSFET. Reduce b, d can significantly reduce the oscillation amplitude. To prove the dependence of the oscillation amplitude on b, d. The following experiment is setup. In the experiment, b slope is kept constant which can be set by using the same R_{gon}. And the d slope is changed by using different V_{gsoff}.

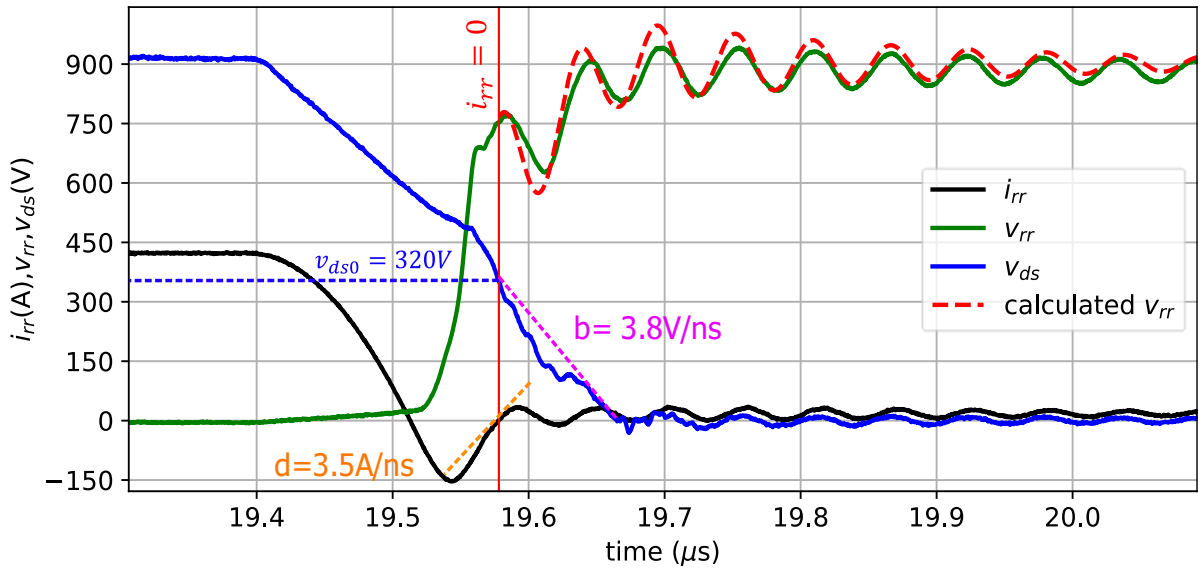


Figure 5.10: *Case 2: R_{gon} = 4.7 Ω, R_{goff} = 2.2 Ω, V_{gsoff} = -2V, V_{gson} = 15V, fitting the calculated model (red dashed line) to the measurement result (green line).*

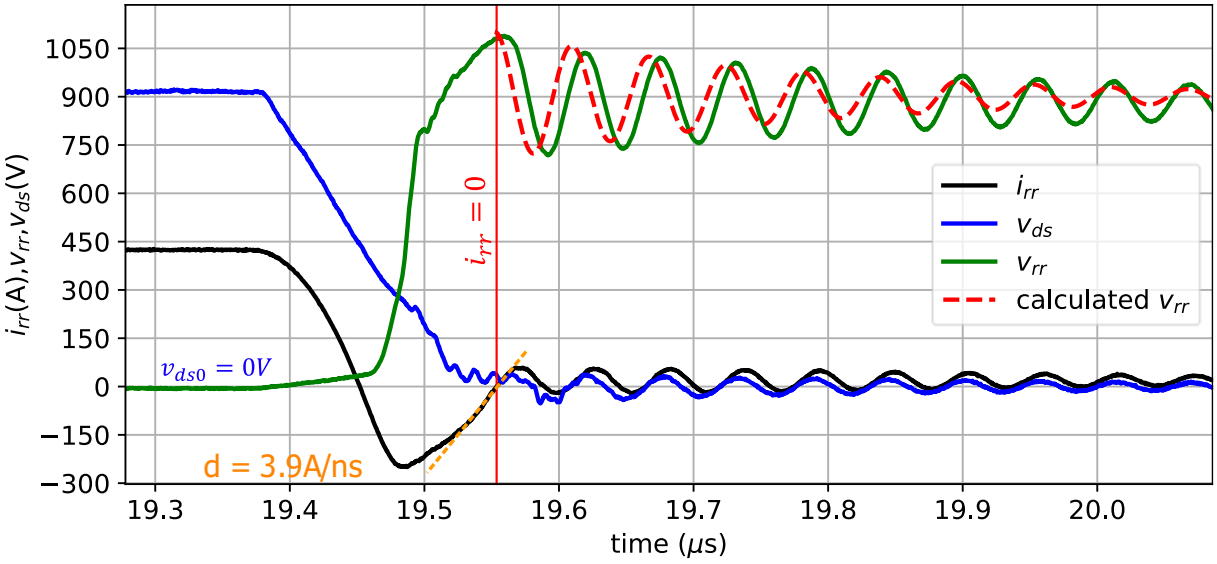


Figure 5.11: *Case 3: R_{gon} = 2.2 Ω, R_{goff} = 2.2 Ω, V_{gsoff} = -2V, V_{gson} = 15V fitting calculated model (red dashed line) to the measurement result (green line).*

When the upper MOSFET is off at higher turn-off gate voltage, the parasitic turn-on happens easier, when the channel of the MOSFET is opened, the short-circuit current is added to the total reverse-recovery current. Consequently, the reverse-recovery current slope is softer. It should be noticed that the falling voltage slope *b* is independent from the gate's turn-off voltage V_{gsoff}.

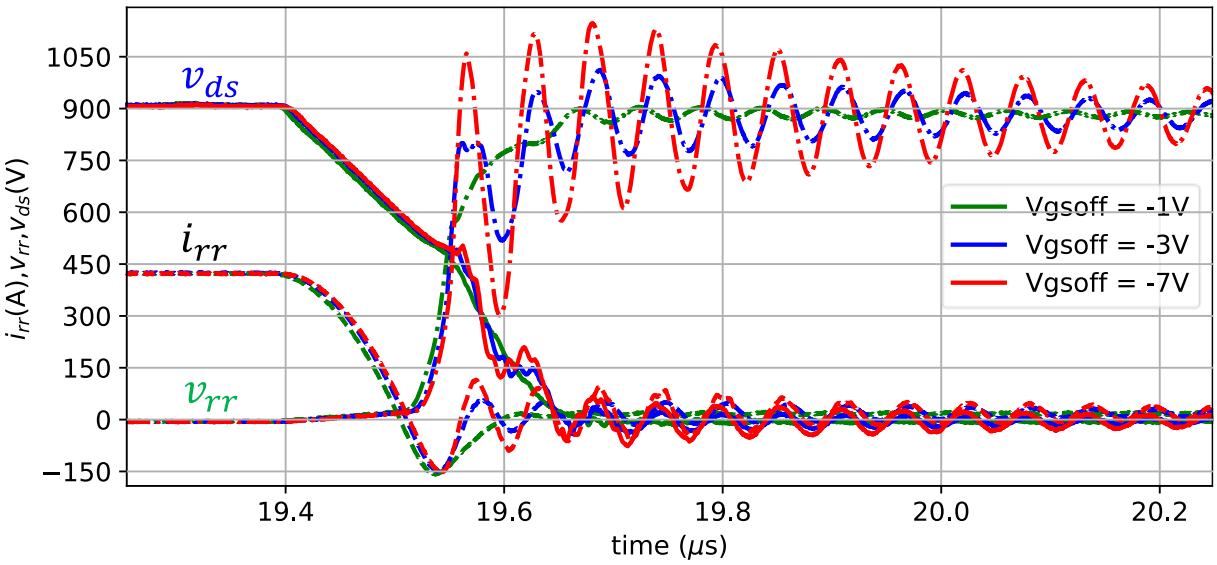


Figure 5.12: *Reverse-recovery waveforms with different turn-off gate voltages and the same gate resistances: R_{gon} = 4.7Ω. The voltage slopes b are similar. The oscillation amplitudes are smaller when the reverse-recovery current slope d is slower.*

Figure 5.12 shows the reverse-recovery waveforms of the upper MOSFET at different turn-off gate voltages -1V (green), -3V (blue), -7V (red) with the same gate resistances: R_{gon} = 4.7Ω, R_{goff} = 2.2 Ω. If the lower index 1, 3, 7 are used correspondingly for the turn-off voltage -1V, -3V, -7V. It can be seen in Figure 5.12 that the slope $d_1 < d_3 < d_7$ and $b_1 = b_3 = b_7$ (same R_{gon}). From the equations (5.29), (5.31), (5.32), the oscillation amplitudes depend on d, b and they can be estimated that $A_1 < A_3 < A_7$. The estimated results are confirmed by the measurement, which can be seen in Figure 5.12. With the same voltage slope b, the oscillation amplitude is smaller when the current slope d is softer.

As can be seen that V_{gsoff} can control d slope with parasitic turn-on effect, R_{gon} can control b slope. Perhaps, it is possible to tune V_{gsoff} and R_{gon} to get the minimum overvoltage and low reverse-recovery energy. Because the oscillation amplitude is equal $A = \sqrt{c_1^2 + c_2^2}$, the minimum of A can be:

- If $b = 0$, $A_{min} = c_2 = \frac{d_{min}}{\omega}$ can be achieved with the minimum of the d slope

- If $b \neq 0$, A_{min} can be achieved when c_1, c_2 have their minimum values. c_{1min} is at the lowest possible b_{min} slope. And the minimum of c_2 is zero, it can be achieved by adjusting d equal to:

$$d + \alpha b_{min} C_{oss} = 0 \tag{5.42}$$

$$\rightarrow \frac{d}{b_{min}} = \frac{-R_2 C_{oss}}{2L_2}$$

Reducing d, b can lower the oscillation on the MOSFET but there is always a trade-off between high reverse-recovery losses and less oscillation, less overvoltage. To find the optimal d, b value for low overvoltage and minimum turn-on, reverse-recovery losses, the R_{gon} and V_{gsoff} are changed to find the best combination.

5.4.2 Different cases of the reverse-recovery overvoltage.

The reverse-recovery voltage can be modeled by the equation (5.36). Depending on turn-on switching speed and the commutation loop stray inductance, v_{ds} of T32 can return to zero before or after $t = 0$.

Case1: v_{ds} returns to zero before $t = 0 \rightarrow b = 0, v_{ds0} = 0$, replace to the equation (5.36)

$$v_{rr}(t) = V_{DC}/2 + \frac{d}{\omega} \cdot e^{-\alpha t} \cdot \sqrt{L_2/C_{oss}} \cdot \sin\left(\omega t + \frac{\pi}{2} + \varphi\right) \tag{5.43}$$

The maximum of the reverse-recovery voltage can be:

$$V_{rrmax} \approx V_{DC}/2 + \frac{d}{\omega} \cdot \sqrt{\frac{L_2}{C_{oss}}} = V_{DC}/2 + L_2 d \tag{5.44}$$

The overvoltage is driven by the commutation loop's inductance L_2 and the reverse-recovery current slope d, it happens at $t = 0$, and $\varphi = -\arctan\left(\frac{R_2}{2}\sqrt{\frac{C_{oss}}{L_2}}\right) \approx 0$.

Case 2: v_{ds} returns to zero after $t = 0 \rightarrow b \neq 0, v_{ds0} \neq 0$, the maximum reverse-recovery voltage:

$$V_{rrmax} = Max(V_{DC}/2 - v_{ds0} - bR_2C_{oss} + bt) + Max\left(A \cdot e^{-\alpha t} \cdot \sqrt{L_2/C_{oss}} \cdot \sin(\omega t - \theta + \varphi)\right) \quad (5.45)$$

$$V_{rrmax} \approx V_{DC}/2 + A\sqrt{L_2/C_{oss}} \quad (5.46)$$

The maximum reverse-recovery voltage in case 2 happens at $t > 0$. It can be seen that in case 1, the overvoltage only depends on the reverse-recovery current slope d, controlling d can limit the overvoltage. In case 2, the overvoltage depends on the oscillation amplitude which is the combination of d and b slope, controlling only d slope can't limit the overvoltage (Figure 5.13).

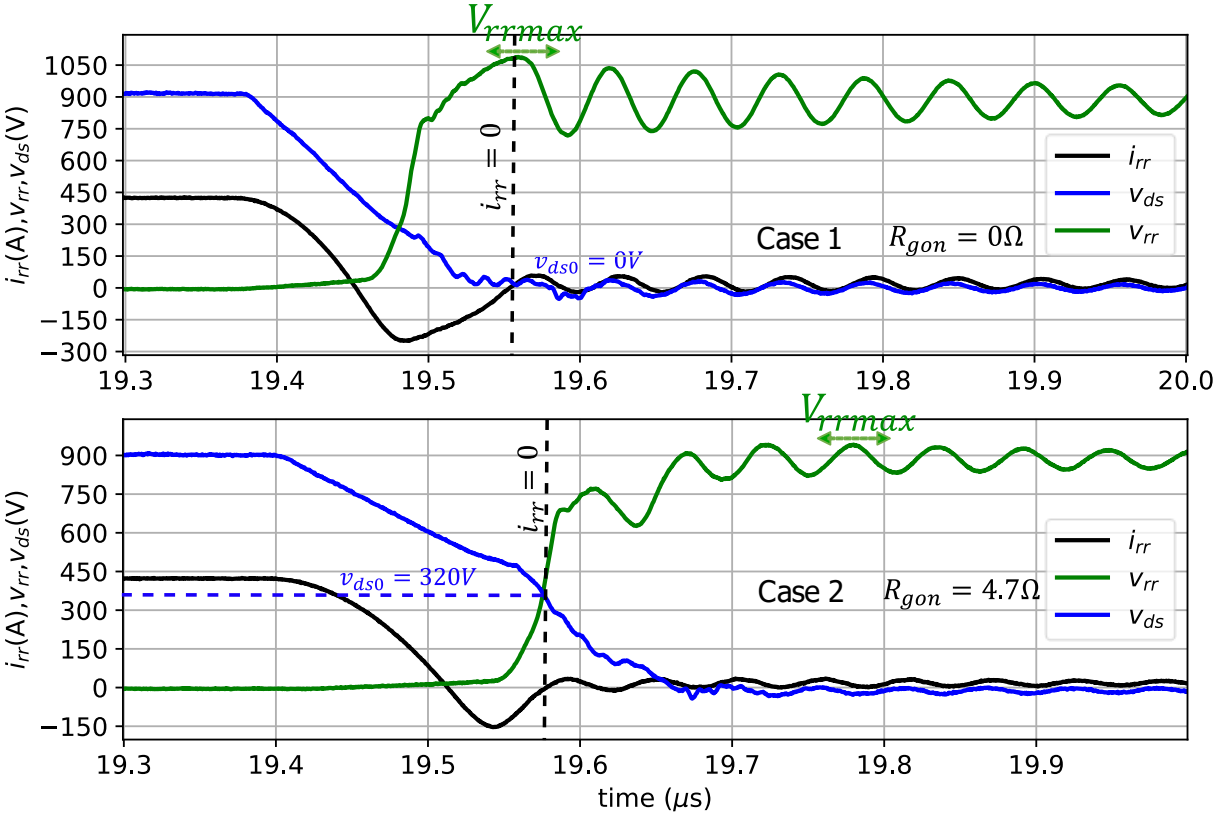


Figure 5.13: *The maximum reverse-recovery overvoltage V_{rrmax} in case 1 and case 2.*

5.4.3 Reverse-recovery overvoltage protection

The equation (5.36) shows that if the lower MOSFET's voltage v_{ds} returns to zero before the reverse-recovery current (case 1), it is possible to limit the upper body's diode overvoltage by controlling only the slope d of the reverse-recovery current. As discussed in previous

section, it has been demonstrated that parasitic turn-on can softer the reverse-recovery current simply by increasing the turn-off gate voltage.

When the active clamping is implemented for the upper MOSFET, if the body diode's voltage is larger than the breakdown voltage of the clamping diode' chain, the upper MOSFET's gate is charged with the diode's breakdown current. By adjusting V_{gsoff} in such a way that the gate voltage can rise above the threshold voltage during the breakdown, the more the overvoltage is, the more the gate voltage is pulled up, resulting in a softer slope of the reverse-recovery current. Consequently, the overvoltage is effectively clamped. It should be noted that there are two feedback loops involved in the reverse-recovery process as can be seen in the Figure 5.14. One is the parasitic turn-on and another is the active clamping.

The main difference between the parasitic turn-on (PTO) and the active clamping is the feedback signal. The parasitic turn-on feeds back only the $\frac{dv_{rr}}{dt}$ while the active clamping feeds back both the overvoltage V_{rrmax} and $\frac{dv_{rr}}{dt}$ (Figure 5.14).

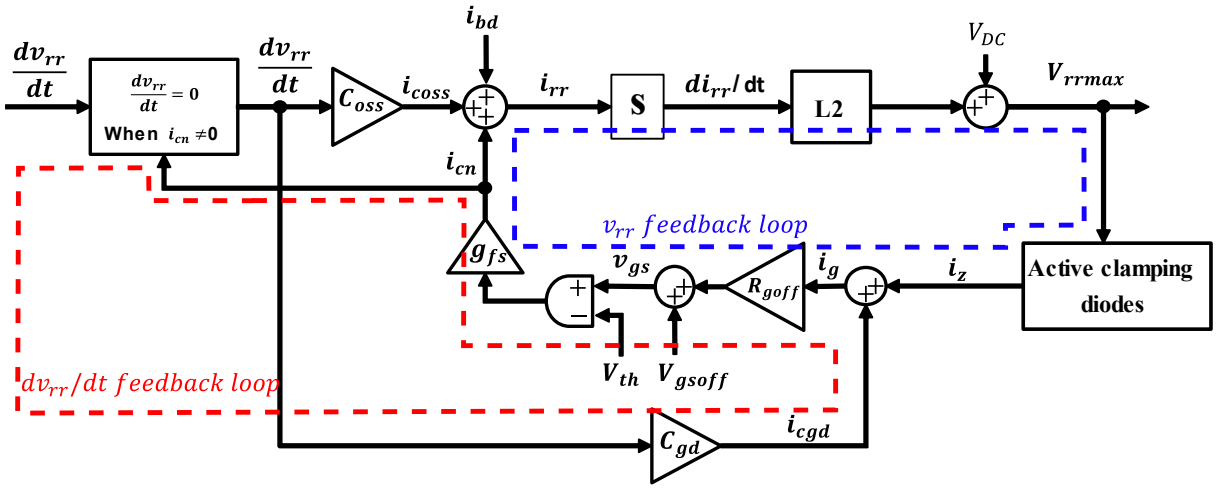


Figure 5.14: *Feedback control loops of active clamping (dashed blue line) and parasitic turn-on (dashed red line) in case 1.*

The difference can be observed in Figure 5.15 which is measured at the same switching conditions: V_{DC} = 1800V, IL= 600A, R_{gon} = 0Ω, R_{goff}=5.1 Ω, T_j = 150°C. The MOSFET T31 is turned off at V_{gsoff} = -5V. The breakdown voltage of the TVS diodes is 1020V, the threshold voltage at T_j = 150°C is around 3.15V. In Figure 5.15, at t_1, the gate voltage, v_{gs1}, rises above

the threshold voltage for both cases, the channel is on and it clamps $\frac{dv_{rr}}{dt}$ to 0. However, the crucial difference between two cases is at t_2. In the case of parasitic turn-on (PTO), v_{rr} slowly rises again, but the $\frac{dv_{rr}}{dt}$ after t_2 is insufficient to turn on the channel once more time, resulting in the overvoltage not being clamped. In the active clamping scenario, apart from the $\frac{dv_{rr}}{dt}$ feedback loop, the overvoltage is also feedback to the gate by the TVS diodes, which makes it more effective to clamp v_{rr}.

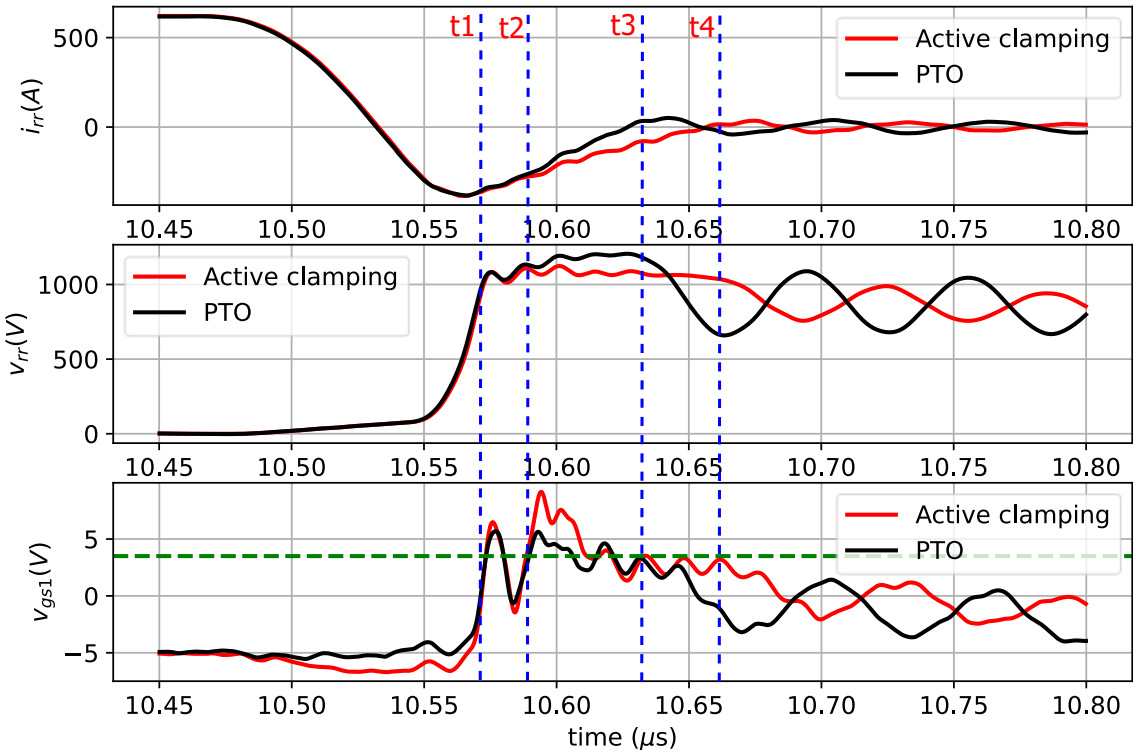


Figure 5.15: *The difference between the active clamping (red lines) and parasitic turn-on (black lines) during the reverse-recovery.* V_{DC} *= 1800V, IL= 600A,* R_{gon} *= 0Ω,* R_{goff} *=5.1 Ω,* T_j *= 150°C,* V_{gsoff} *= -5V,* V_{TVS} *= 1020V,* V_{th} *= 3.15V.*

5.5 Turn-on losses optimization

The previous sections show the ability to clamp the reverse-recovery overvoltage with the parasitic turn-on effect and the active clamping circuit simply by adjusting the turn-off gate voltage V_{gsoff}. Even though the method adds more reverse-recovery losses but the turn-on losses can be further reduced with the smaller R_{gon}. Finding the optimal values for R_{gon} and V_{gsoff} is

crucial to minimize total turn-on and reverse-recovery losses while maintaining safe overvoltage levels.

5.5.1 Optimization method

The method has two main control parameters: R_{gon} and V_{gsoff}. R_{goff} can be considered as an independent variable which are selected from the turn-off gate resistor tuning process. The first step would be finding the suitable range of R_{gon} and V_{gsoff}, in which they are discretized into discrete values. Each discrete combination of the R_{gon} and V_{gsoff} is a candidate for the optimal selection. All the candidates will be measured at the worst-case scenario conditions which are at the maximum V_{DC}, maximum load current and maximum junction temperature. The overvoltage and the total turn-on and reverse-recovery losses are recoded and compared to select the best combination.

To demonstrate the optimization method, the double pulse test is set up for the hybrid ANPC. The R_{gon} is discretized in range [0, 1.2, 2.2, 3.3, 4.3, 5.6] Ω and V_{gsoff} is discretized in range [-7, -5, -3, -2, -1, 0] V. The measurements are made at V_{DC}= 1800V, IL = 600A, T_j = 150°C. The turn-off gate resistor R_{goff} is selected at 5.1Ω. Three different scenarios are measured:

Case 1: Parasitic turn-on (PTO)

Case 2: Active clamping (ACL)

Case 3: Active clamping together with the dual soft ferrite cores (ACL_FR).

To select the best candidate, the overvoltage should have higher priority than the losses. For that reason, the overvoltage is plotted over R_{gon} in the Figure 5.17 and over V_{gsoff} in the Figure 5.16.

The conventional R_{gon} tuning method (no parasitic turn-on or active clamping) chooses R_{gon} = 4.3Ω and V_{gsoff} = -7V to limit the overvoltage during reverse-recovery to 1175V. The total turn-on and reverse-recovery losses are at 37mJ.

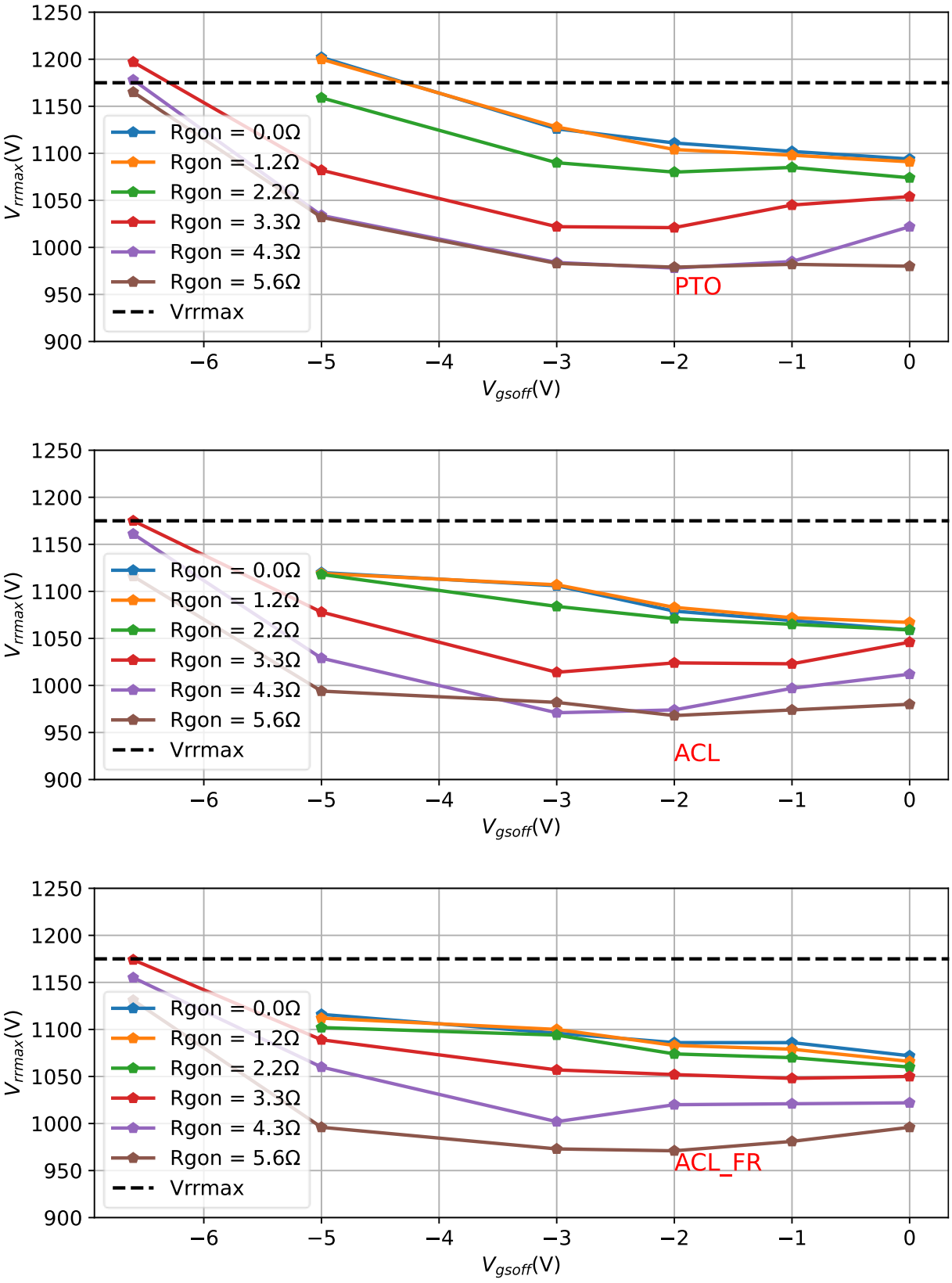


Figure 5.16: *Reverse-recovery overvoltage over the V_{gsoff} for 3 different cases, at V_{DC}= 1800V, IL = 600A, T_j = 150°C, R_{goff} = 5.1Ω.*

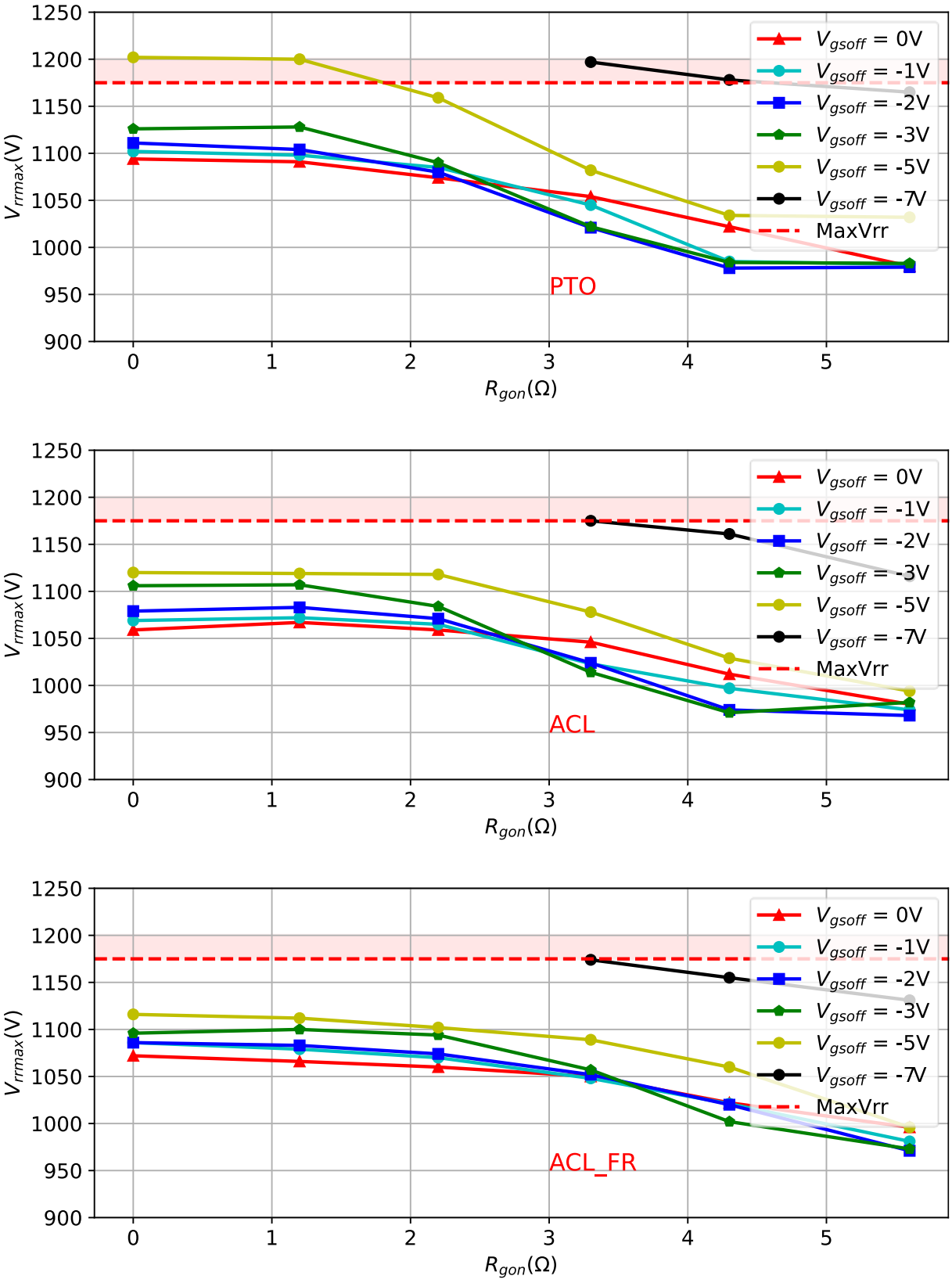


Figure 5.17: *Reverse-recovery overvoltage over the R_{gon} for 3 different cases, at V_{DC}= 1800V, IL = 600A, T_j = 150°C, R_{goff} = 5.1*

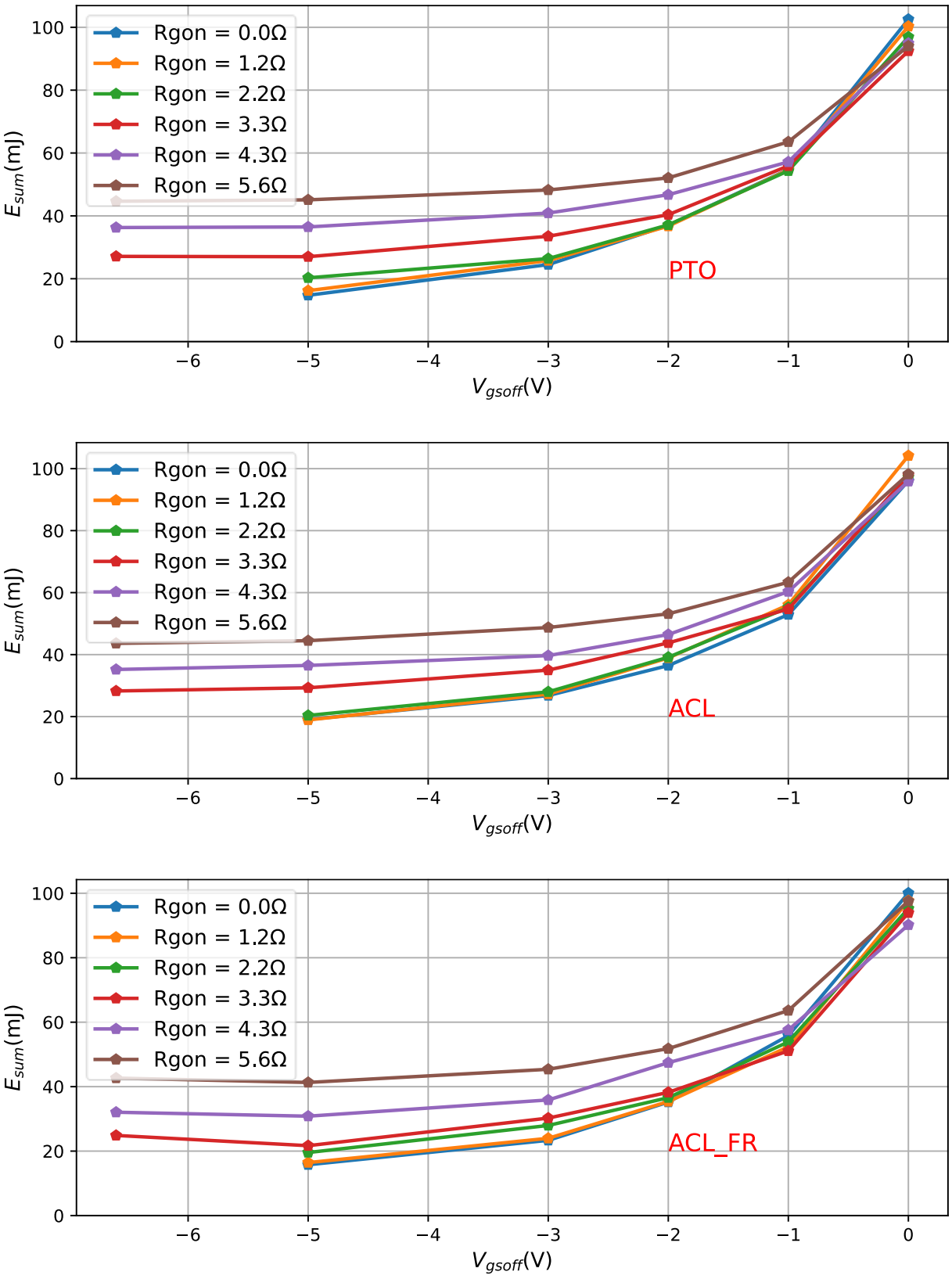


Figure 5.18: *The total turn-on losses over the V_{gsoff} for 3 different cases, at V_{DC}= 1800V, IL = 600A, T_j = 150°C, R_{goff} = 5.1Ω*

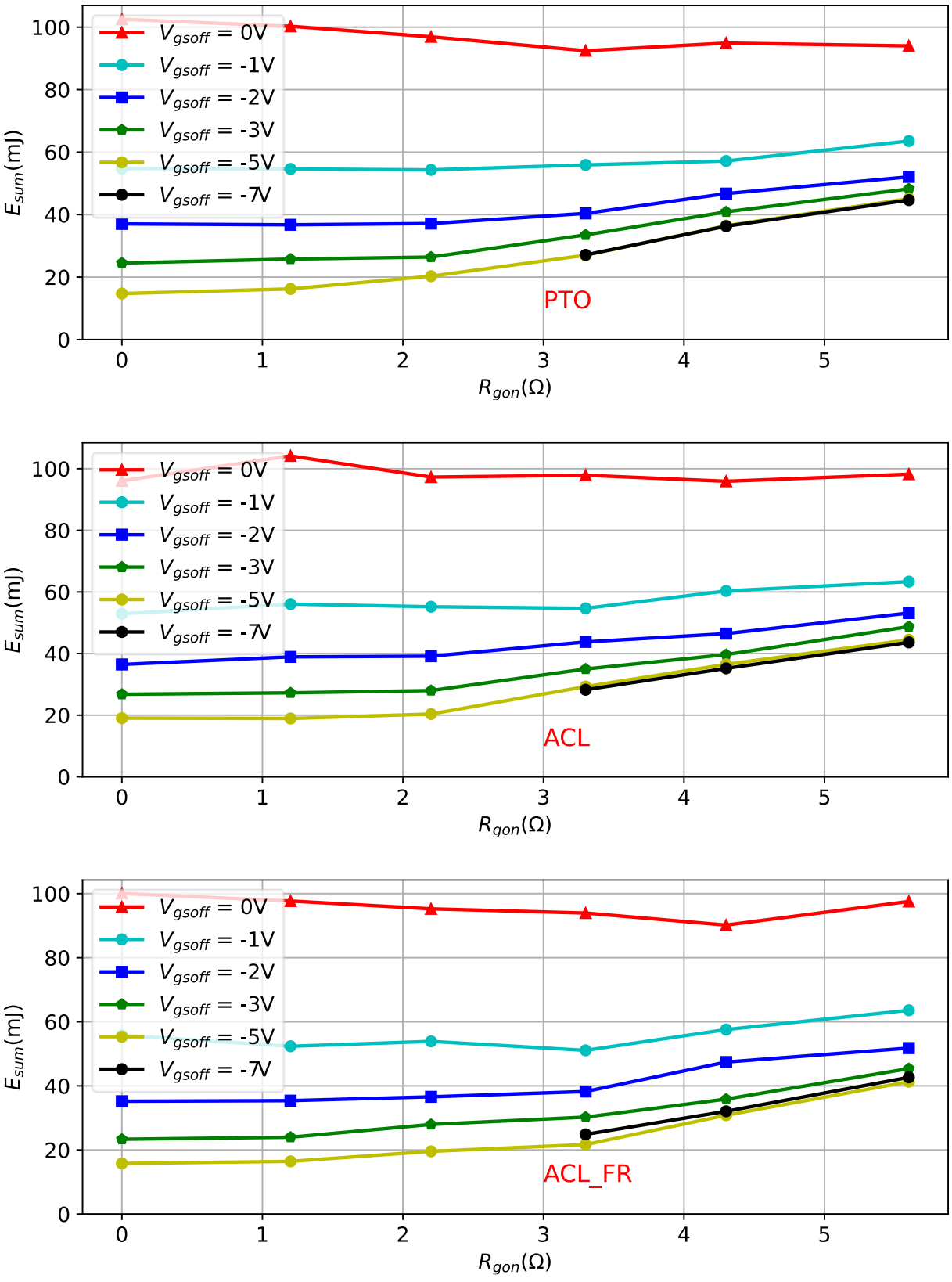


Figure 5.19: *The total turn-on losses over the R_{gon} for 3 different cases, at V_{DC}= 1800V, IL = 600A, T_j = 150°C, R_{goff} = 5.1Ω*

The Figure 5.17 shows that:

- At very low turn-off gate voltage (V_{gsoff} = -7V), there is no parasitic turn on, the lowest R_{gon} can be selected is 4.3 Ω to limit the overvoltage to V_{rrmax} = 1175V.
- When the turn-off gate voltage slightly increases to -5V, the parasitic turn-on has some effects on reducing the oscillation and overvoltage, R_{gon} now can be reduced up to 2.2 Ω without over the voltage limit.
- If the active clamping is used, the clamping effect can be seen even at V_{gsoff} = -5V when R_{gon} is reduced below 2.2Ω.

Figure 5.19 illustrates that, across all three cases, having V_{gsoff} set to -5V results in the lowest combined turn-on and reverse-recovery losses. Remarkably, the total losses in all three cases are very close and approximately 20mJ which is 46% lower than conventional tuning method at 4.3Ω and -7V. The significant difference between these cases is indeed the range of R_{gon} values that can be selected or how fast the turn-on speed can be increased without over the voltage limit. When only relying on the parasitic turn-on (PTO) effect, an optimal choice for R_{gon} is approximately 2.2Ω. In contrast, when an active clamping is implemented, R_{gon} can be selected at 0 Ω, 1.2 Ω, 2.2Ω. Furthermore, when ferrite cores are used into the circuit, the range of suitable R_{gon} is 0Ω, 1.2 Ω, 2.2Ω, 3.3Ω. The optimal R_{gon} is chosen at 2.2Ω to limit the MOSFET's overshoot current under 900A.

Figure 5.20 depicts the differences in the voltages and currents waveforms of the above scenarios at the same switching conditions: V_{gsoff} = -5V and R_{gon} = 2.2Ω, R_{goff} = 5.1Ω V_{DC}= 1800V, IL = 600A, Tj = 150°C. Some major differences can be pointed out:

- When ferrite cores are used in ACL_FR, the high frequency oscillation is effectively removed.
- The overvoltage is clamped when the active clamping is employed (ACL, ACL_FR).
- In case of ACL_FR, the voltage drop during the turn-on is slightly faster due to the cores' inductance.

The above experiments demonstrate that parasitic turn-on during the reverse-recovery of the body diode can benefit low turn-on losses and safe clamped overvoltage if R_{gon} and V_{gsoff} are carefully selected.

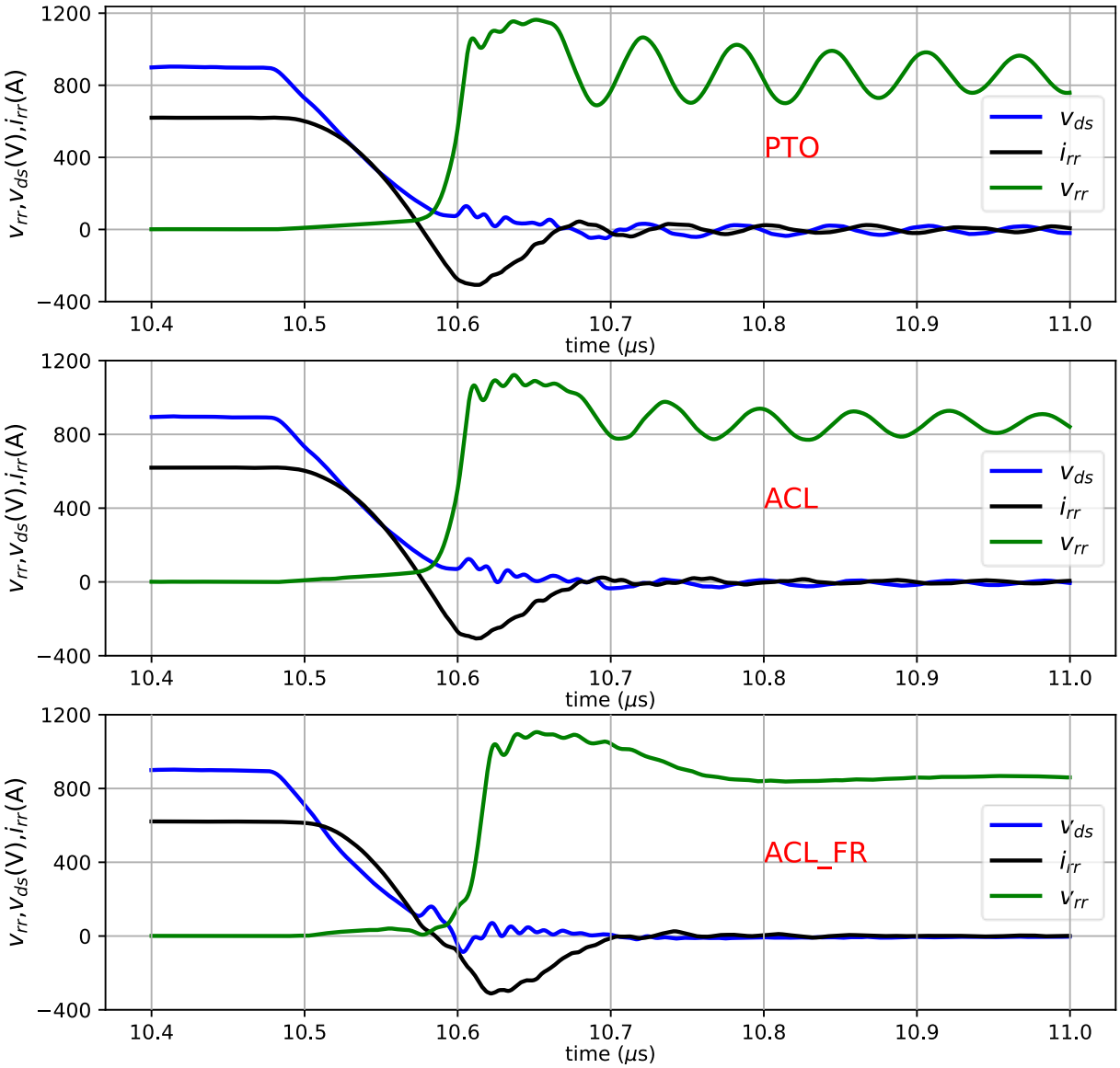


Figure 5.20: *Reverse-recovery waveforms at V_{gsoff} = -5V and R_{gon} = 2.2Ω, R_{goff} = 5.1Ω V_{DC}= 1800V, IL = 600A, Tj = 150°C in 3 cases: PTO: parasitic turn-on, ACL: active clamping, ACL FR: active clamping and dual ferrite cores.*

5.5.2 The variation of threshold voltage and the turn-off voltage sensitivity.

One of the important conditions to apply the active clamping and parasitic turn-on effect is the threshold voltage of the device. It is well known in literatures that the threshold voltage is changed at different temperature like in the Figure 5.21 or when the module is aged [106, 107, 108, 109, 110] or the parameters variation in series production. All the results presented in the previous sections were obtained at a junction temperature of 150°C. At lower

temperatures, the threshold voltage tends to be higher (Figure 5.21). Consequently, the total losses at lower temperatures are expected to be lower compared to higher temperatures due to the reduction in reverse-recovery charge and overshoot current.

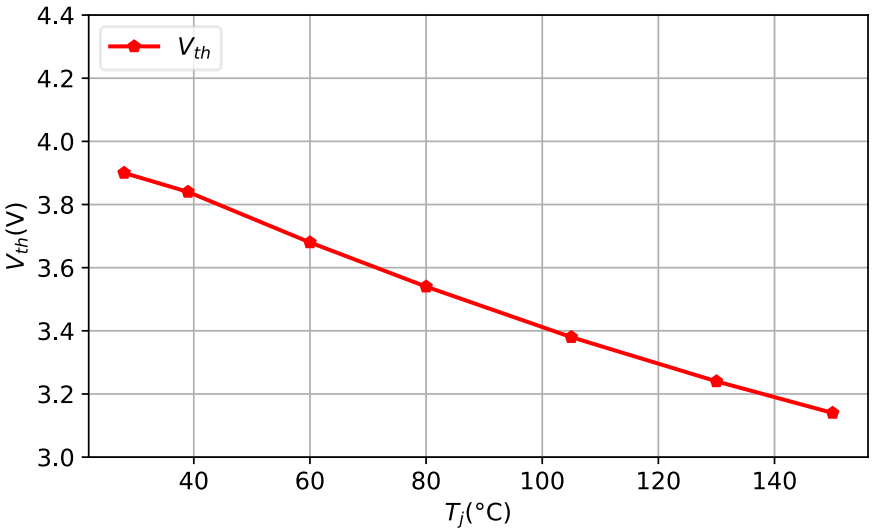


Figure 5.21: *The variation of FF3MR12KM1P MOSFET's threshold voltage against the junction temperature.*

However, a crucial concern arises when operating at lower temperatures. The effectiveness of the active clamping, particularly its ability to clamp the overvoltage with a -5V turn-off gate voltage, becomes uncertain. This raises questions about overvoltage protection, as it's unclear whether the active clamping will still perform as expected in these conditions. To investigate further on this issue, the threshold voltage of a brand new SiC MOSFET FF3MR12KM1P module is measured at different junction temperatures as depicted in the Figure 5.21. The threshold voltage at 150°C is 3.15V and it is expected to increase up to 4.0V at 0°C. In term of parasitic turn-on, an increase or decrease in the threshold voltage will have the same effect as increase or decrease the turn-off gate voltage when we assume that the dead time is long enough. For example, if at 150°C junction temperature, the threshold voltage is 3.15V and the parasitic turn-on happens at V_{gsoff} = -5V. At zero junction temperature, the threshold voltage increases 0.85V, it is possible to increase the turn-off gate voltage correspondently 0.85V to have the same parasitic turn-on effect. This means at T_j = 0°C, and V_{gsoff} = -4.15V will have the same parasitic turn-on with T_j = 150°C and V_{gsoff} = -5V.

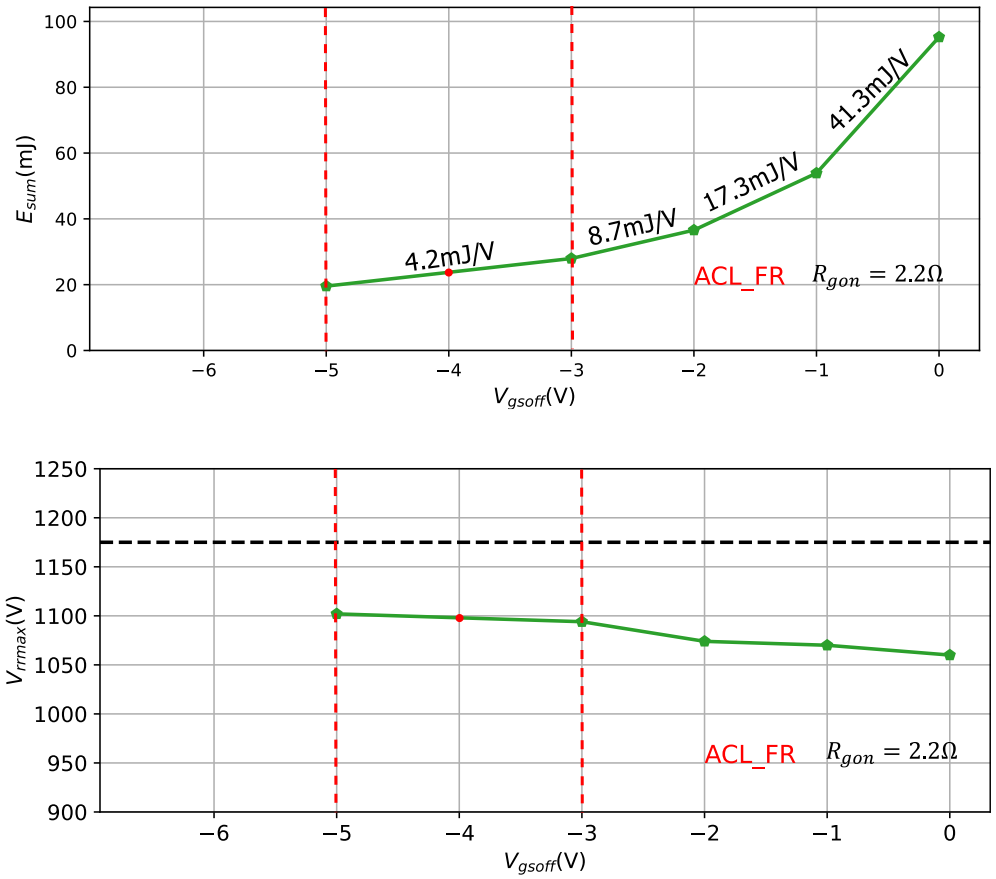


Figure 5.22: *The total turn-on losses E_{sum} a) and the reverse-recovery overvoltage V_{rrmax} b) in case of R_{gon} = 2.2Ω when the active clamping and ferrite cores (ACL-FR) are used. V_{DC}= 1800V, IL = 600A, T_j = 150°C, R_{goff} = 5.1Ω.*

It can be observed in the Figure 5.22 that in case of active clamping and ferrite cores are used (ACL_FR), both E_{sum} and V_{rrmax} has the lowest sensitivity with V_{gsoff} in range $-5V \leq V_{gsoff} \leq -3V$. When the optimal point R_{gon} = 2.2Ω and V_{gsoff} = -4 V is chosen, it ensures the reverse-recovery overvoltage V_{rrmax} stay around the optimal value with the variation of threshold voltage ±1V. When the junction temperature changes from 0°C to 150°C, the overvoltage is maintained at 1100V and the total losses have minor changes due to its V_{gsoff} is in low sensitivity region. In other cases: only parasitic turn-on (PTO) or with only the active clamping (ACL), the optimal V_{gsoff} regions may be different. There is possibility that the lowest sensitivity regions of E_{sum} and V_{rrmax} have no common V_{gsoff} values. In this situation, the low sensitivity region of V_{rrmax} should be given higher priority.

5.6 Compare total turn-on losses in different situations

To have an overview of the total turn-on and reverse-recovery losses (E_{sum}) of SiC MOSFET in different situations, the double pulse test for the SiC MOSFET was set up. To avoid the complex scenarios and make it simple to compare, the active clamping was not used in this comparison and the turn-off gate resistor is fixed at 50Ω for all experiments. The experiment conditions: V_{DC} = 1500V, T_j =25°C.

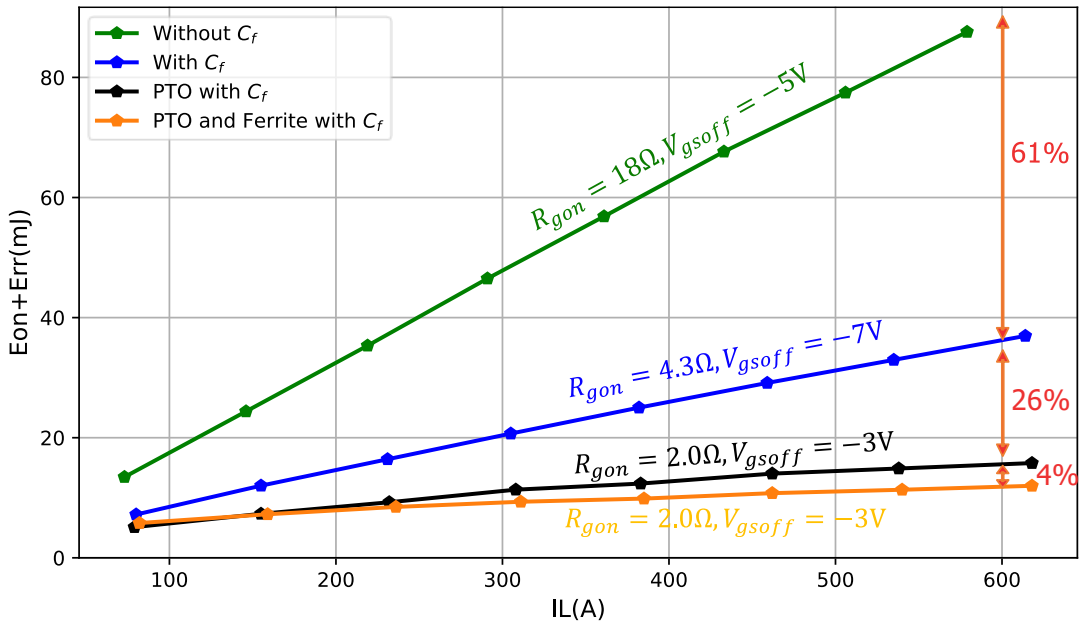


Figure 5.23: *Compare the total turn-on losses in different scenarios,* V_{DC} = 1500V, 25°C.

Case 1: Conventional method without C_f. When there is no decoupling capacitor C_f, because of the large commutation circuit's inductance, by conventional tuning R_{gon} method, the smallest R_{gon} can get is 18 Ω to limit the overvoltage at 1175V. The MOSFET is turned on at slow speed and hence high turn-on losses (green line).

Case 2: C_f. When there is decoupling capacitor C_f, the commutation loop is now smaller, the lowest R_{gon} with the conventional tuning method can be get at 4.3Ω, V_{gsoff} = -7V (blue line). The turn-on losses can be reduced up to 61% compare to case 1 (at IL = 600A).

Case 3: C_f and PTO. When the parasitic turn-on is applied. The V_{gsoff} is selected at -3V and R_{gon} = 2.0 Ω. The overall turn-on losses (black line) is further reduced another 26%(at IL = 600A).

Case 4: C_f, PTO and FR. When the ferrite cores are used, the ferrite cores act as turn-on snubber which can further reduce the turn-on losses. The V_{gsoff} is selected at -3V and R_{gon} = 2.0 Ω (orange line). A reduction by 4% can be seen at IL = 600A. Finally, a total reduction of 91% compare to case 1 can be achieved.

5.7 Compare turn-off losses of different situations

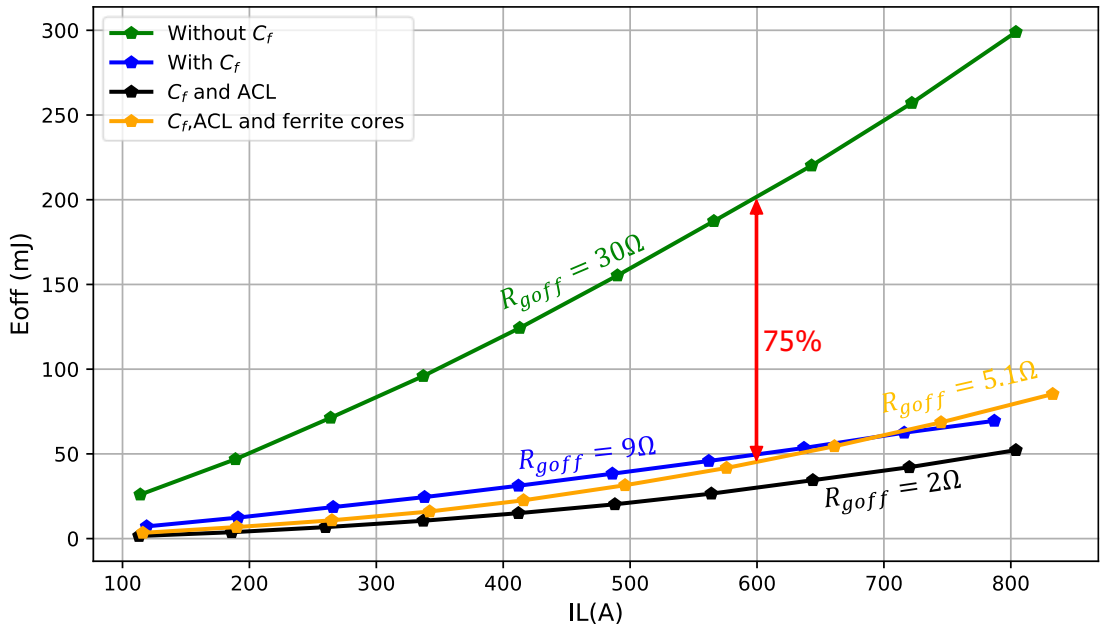


Figure 5.24: *Compare the turn-off losses in different scenarios,* V_{DC} = 1500V, 25°C.

Case 1: Without decoupling capacitor C_f. Because of the large commutation loop, the R_{goff} = 30Ω was chosen to limit the overvoltage on the SiC MOSFET. The turn-off loss is really high (green line).

Case 2: When the decoupling capacitor is used, the minimum R_{goff} was chosen at 9Ω. The turn-off loss (blue line) is significantly reduced up to 75% compare to case 1 because of the smaller commutation loop (at IL = 600A).

Case 3: When the active clamping circuit is implemented, it is possible to increase the turn-off speed, R_{goff} = 2Ω was chosen. The turn-off loss (black line) is further reduced by 10% compare to case 2 (at IL = 600A).

Case 4: When the ferrite cores are used for the oscillation damping, they also introduced more inductance to the commutation loop even with the decoupling capacitor. The turn-off losses (orange line) is slightly higher than case 3 because the R_{goff} is selected at 5.1 Ω to limit the overvoltage of the SiC MOSFET.

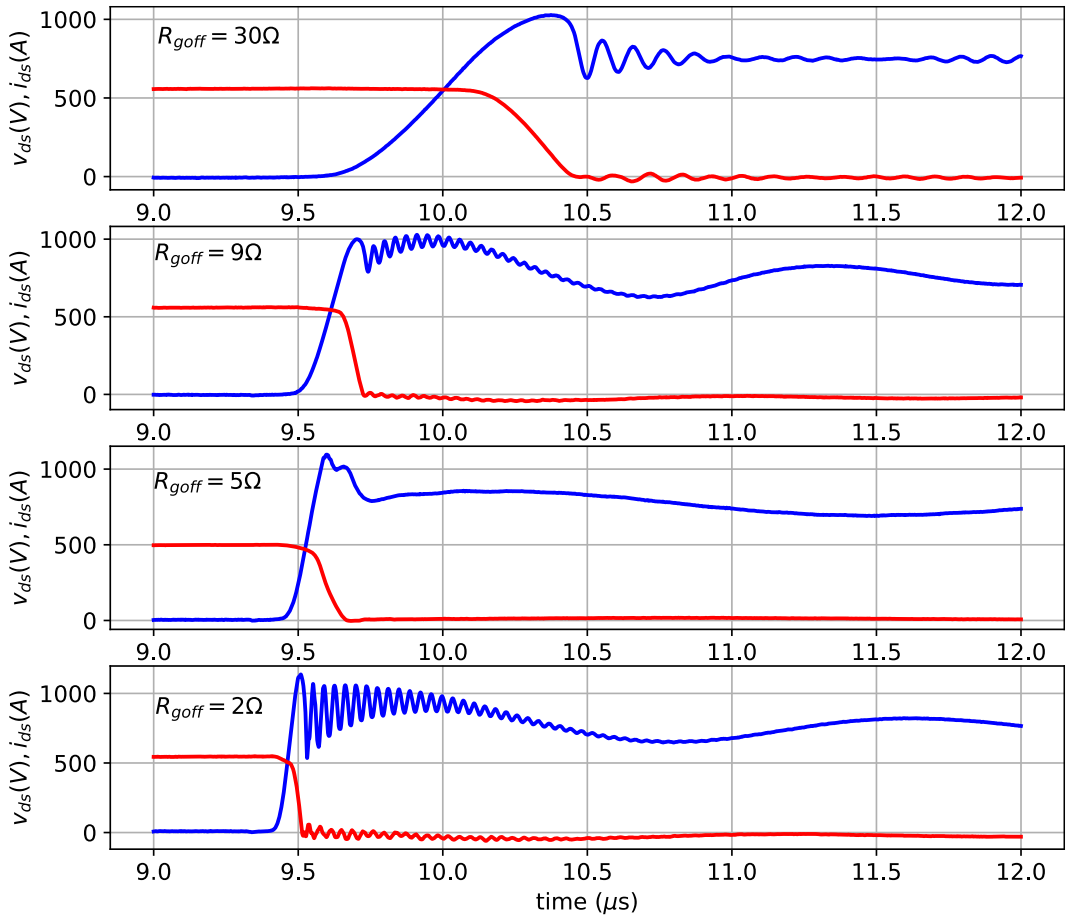


Figure 5.25: *SiC MOSFET's turn-off voltage and current in different cases. V_{DC} = 1500V, 25°C.*

Figure 5.23 and Figure 5.24 have demonstrated the importance of the decoupling capacitor in this 2SiC hybrid ANPC topology. Since it can reduce the turn-on losses by 61% and the turn-off losses by 75% compare to a normal 2SiC hybrid ANPC. Without decoupling capacitor, SiC MOSFETs have no longer low switching losses at high switching frequency because they have to reduce their switching speed to avoid overvoltage.

In summary, the parasitic turn-on effect can be used to soften the reverse-recovery current slope, resulting reduced oscillation and overvoltage. The optimal combination of V_{gsoff} and R_{gon}

can be selected within the low-sensitive region of V_{gsoff} to archive low sensitive overvoltage and total turn-on losses during the variation of SiC MOSFET's threshold voltage.

The analytical model of the reverse-recovery oscillation and overvoltage indicates that the oscillation amplitude depends on the reverse-recovery current slope and the turn-on voltage slope. When rapidly reducing the turn-on voltage before the reverse-recovery current returns to zero, the overvoltage is primarily influenced by the reverse-recovery current slope. Active clamping diodes can be employed to limit the overvoltage in this scenario.

Conversely, when the turn-on voltage is slower than the reverse-recovery current returns to zero, the overvoltage is governed by the oscillation amplitude, which is the result of both the reverse-recovery current slope and the turn-on voltage slope. The active clamping diodes can't protect the body diode in this situation.

6. Devices Characterization

Chapter 6 will provide a comprehensive analysis of the switching and conduction losses of SiC MOSFETs and Si IGBTs in the hybrid topology, considering various operating points and switching frequencies. Because of the decoupling capacitor, the switching losses of SiC MOSFETs are similar to those of conventional two-level inverters, allowing for straightforward modeling using PLECS simulation. However, the switching losses on the IGBTs are more complex due to the drifting voltage of the decoupling capacitor, as discussed in Chapter 4. PLECS lacks the capability to model real switching delays and transient times accurately. To accurately model the switching losses on the IGBTs, it is necessary to manually adjust the switching timings and values of the circuit's parasitic components. Fine-tuning these parameters is crucial to align the real capacitor's current and voltage waveforms with the simulation waveforms. Losses are estimated across various operating currents and switching frequencies to provide a comprehensive understanding of the system's performance.

6.1 SiC MOSFET module

6.1.1 Double pulse test setup

To characterize SiC MOSFET module in the hybrid ANPC, a special double pulse test is set up like in the Figure 6.1. Because the upper of the ANPC has longer commutation loop than the lower of the ANPC, the characterization is carried on the upper part as the worst-case scenario. The IGBT T11 and T21 is always on during the experiment. The Rogowski coil RC1 and RC2 measures the current through T32 and T31 correspondently. The oscilloscope's power supply is floating and its ground is referred to the gate's Kelvin source terminal. The T32's voltage is measured by 1:100 passive voltage probe P1 which is connected directly to the AC terminal of the module. Because the 62mm module has no measurement D terminal, there is an inductance $L_d = 9.2nH$ in between the AC terminal and the real drain terminal of T32 chip. A high voltage differential probe P2 is used to measure the T31's voltage, which is referred to the Kevil terminal of the upper MOSFET and T31's DC+ terminal which is also expected to have a small L_d between the measurement point and the real drain terminal of the device. The upper gate voltage is measured with the isolated optical probe P4. The lower T32's gate voltage is measured with passive 1:10 voltage probe P3.

All the devices are maintained at 150°C by a temperature controller. All the measurement probes are calibrated and de-skewed before the experiments. The equipment has sufficient bandwidth for the transient measurement as can be seen in the Table 6.1.

Table 6.1: *Measurement probes' specifications.*

Probe	Signal	Model	Bandwidth (MHz)	Input capacitor (pF)
RC1	$i_{rr}(t)$	CWTMIni50HF6	50	N/A
RC2	$i_{ds}(t)$	CWTMIni50HF6	50	N/A
P1	$v_{ds}(t)$	1PMK PHV1000	400	7.5
P2	$v_{rr}(t)$	Differential HVD3605	100	2.5
P3	$v_{gs2}(t)$	Lecroy PP09	500	9.5
P4	$v_{gs1}(t)$	Optical HVFO 108	150	23

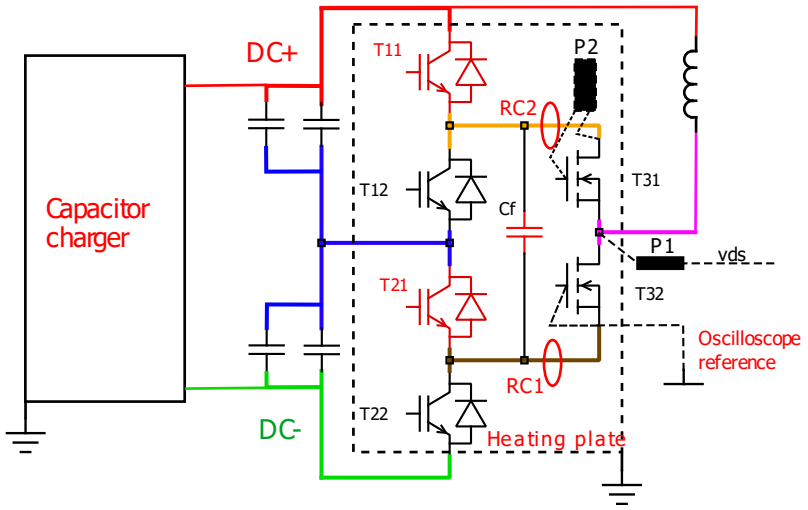


Figure 6.1: *Double pulse test setup for the characterization of the SiC MOSFET.*

The worst-case scenario for the SiC MOSFET switching is defined at: V_{DC} = 1800V, IL = 600A, T_j = 150°C

6.1.2 SiC MOSFET losses in nominal operating conditions

Figure 6.2, Figure 6.3, Figure 6.4 depict the turn-off, turn-on energy and the reverse-recovery energy of SiC MOSFET with V_{gson} = 15V, V_{gsoff} = -4V, R_{gon} = 2.2Ω, R_{goff} = 5.1Ω, TVS' breakdown voltage = 1020V. Ferrite cores are used to damp the switching oscillations.

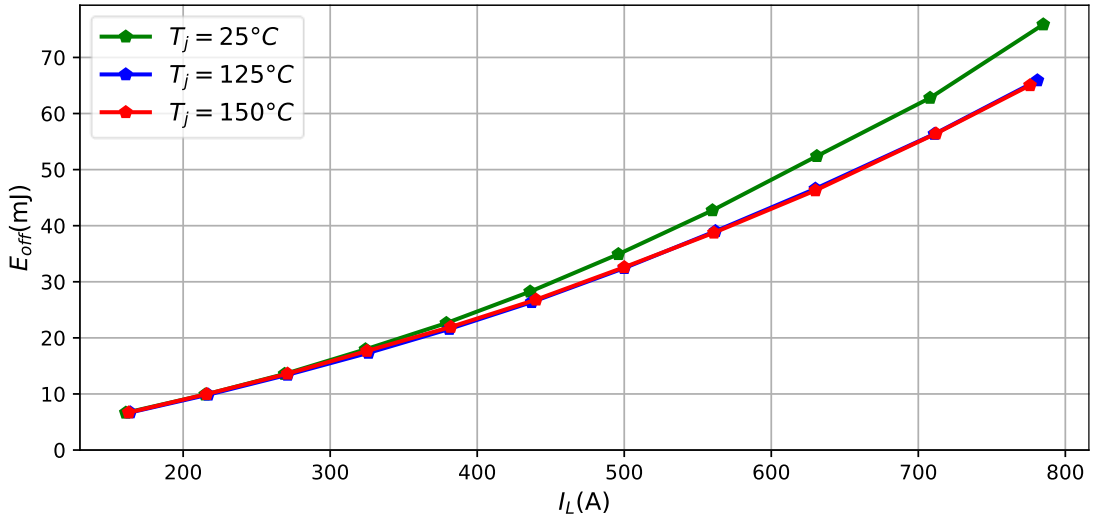


Figure 6.2: *Turn-off losses at different load currents and temperatures. Switching conditions V_{DC} = 1500V, T_j = 25°C, 125°C, 150°C, $L_\sigma = 46nH$, V_{gsoff} = -4V, R_{gon} = 2.2Ω, R_{goff} = 5.1Ω, TVS' breakdown voltage = 1020V.*

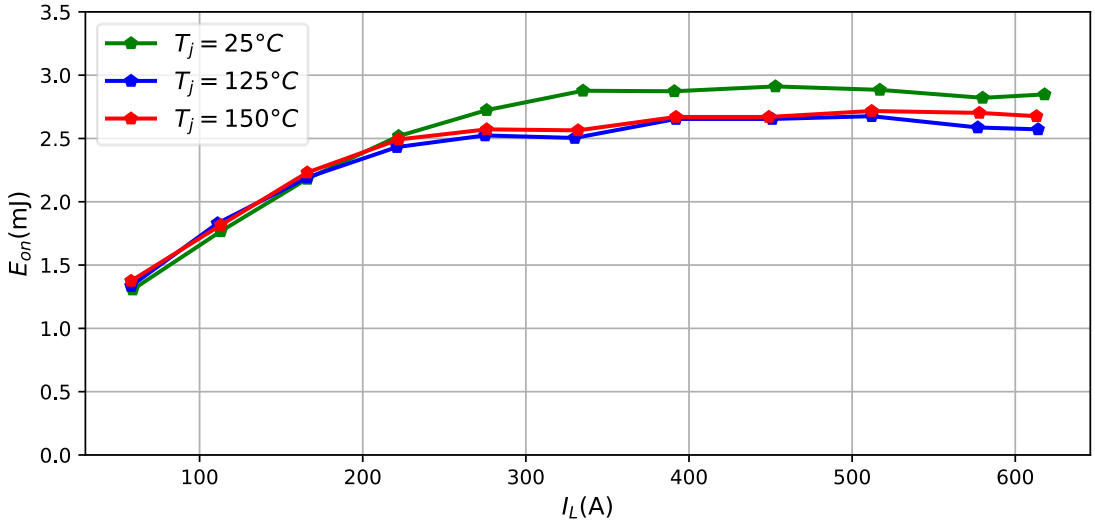


Figure 6.3: *Turn-on losses at different load currents and temperatures. Switching conditions V_{DC} = 1500V, T_j = 25°C, 125°C, 150°C, $L_\sigma = 46nH$, V_{gsoff} = -4V, R_{gon} = 2.2Ω, R_{goff} = 5.1Ω, TVS' breakdown voltage = 1020V.*

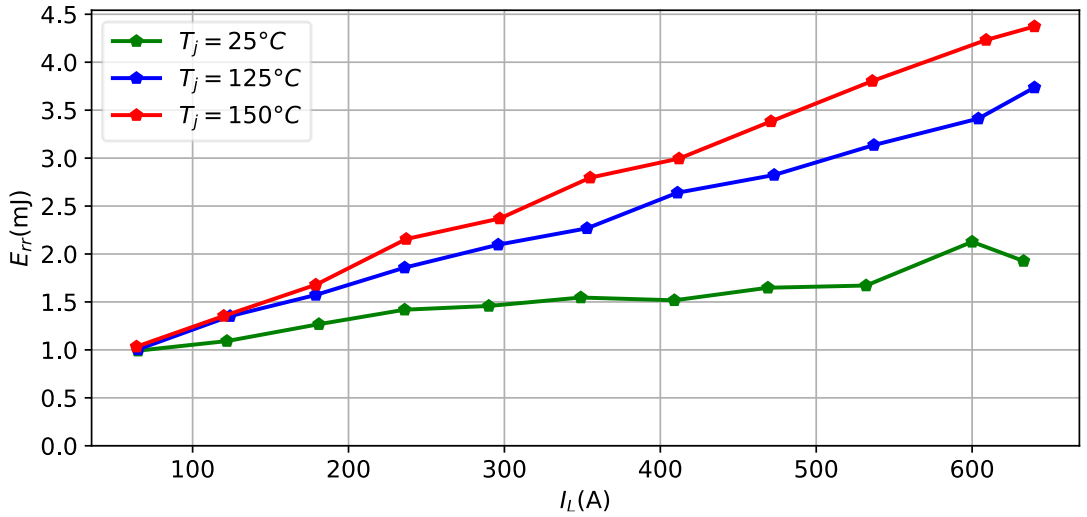


Figure 6.4: *Reverse-recovery losses at different load currents and temperatures. Switching conditions V_{DC} = 1500V, T_j = 25°C, 125°C, 150°C, $L_\sigma = 46nH$, V_{gsoff} = -4V, R_{gon} = 2.2Ω, R_{goff} = 5.1Ω, TVS' breakdown voltage = 1020V.*

6.1.3 Thermal coupling in the double pulse test

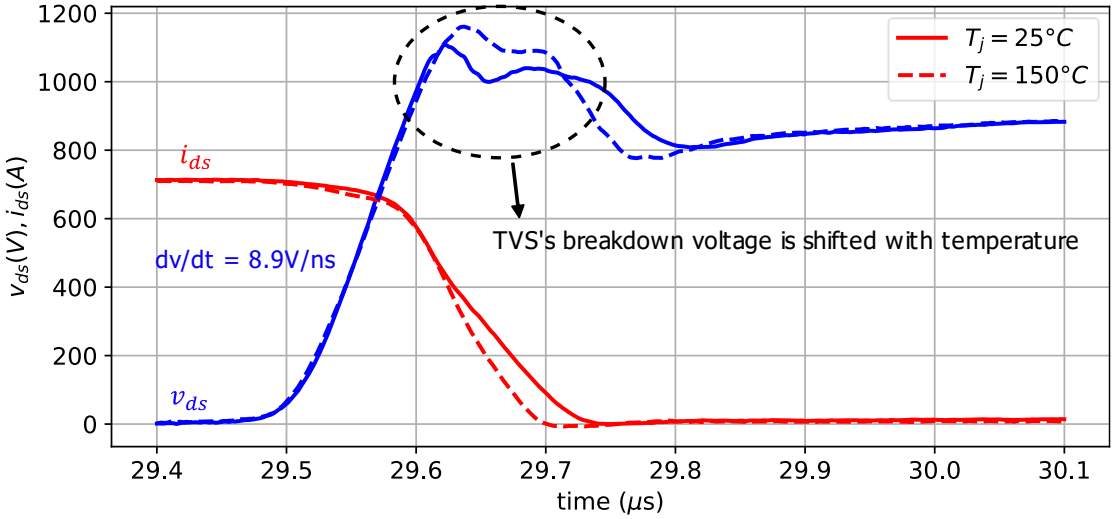


Figure 6.5: *SiC MOSFET's turn-off waveforms. Switching conditions V_{DC} = 1500V, T_j = 25°C (solid lines), 150°C (dashed lines), $L_\sigma = 46nH$, V_{gsoff} = -4V, R_{gon} = 2.2Ω, R_{goff} = 5.1Ω, TVS' breakdown voltage at 25°C = 1000V, TVS' breakdown voltage at 75°C = 1060V, with ferrite cores.*

During the double pulse test, because the active clamping is mounted directly on the SiC MOSFET module and the DC+ and DC- terminal of the module is directly connected to the

TVS string, there is a thermal coupling from the SiC module to the TVS diodes which increase their temperatures up to 75°C when the MOSFET's junction temperature is controlled at 150°C. Consequently, the breakdown voltage of the TVS's diode also increase from 1000V to 1060V (Figure 6.5). The increasing breakdown voltage at high temperature is described in [80, 98]. The effect leads to lower turn-off losses at high temperatures than room temperature which are shown in the Figure 6.2.

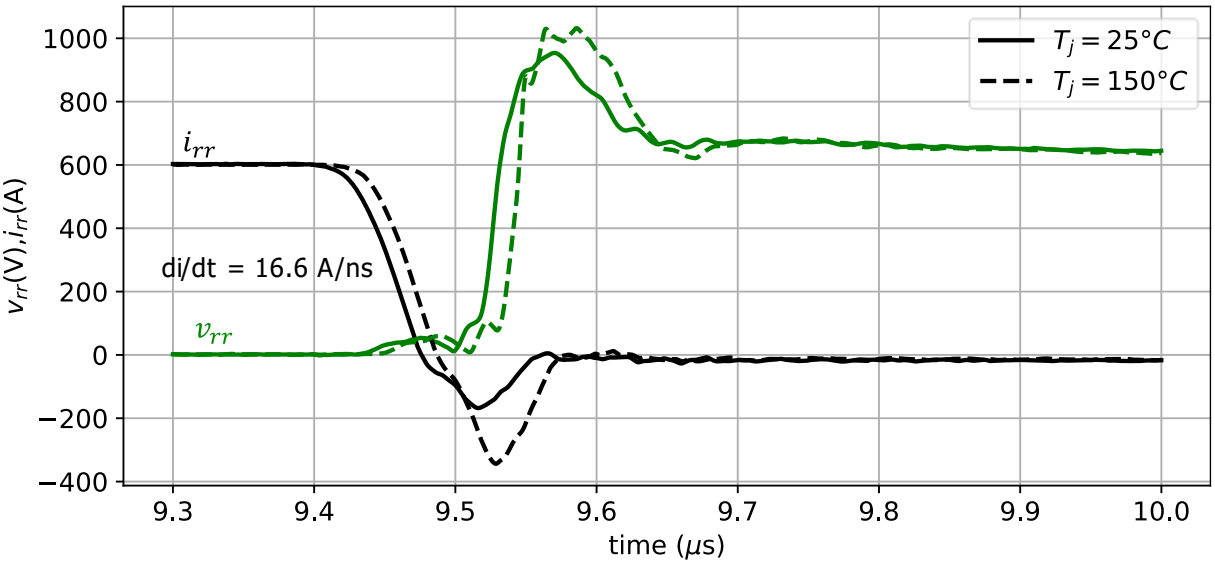


Figure 6.6: *SiC MOSFET's turn-on waveforms. Switching conditions V_{DC} = 1500V, IL =600A, T_j = 25°C (solid lines), 150°C (dashed lines), $L_\sigma = 46nH$, V_{gsoff} = -4V, R_{gon} = 2.2Ω, R_{goff} = 5.1Ω, with ferrite cores.*

6.2 IGBT module

6.2.1 Double pulse test setup

Because of the symmetry between the upper and lower part of the ANPC near to DC link capacitors, the commutation loops of the half-bridge HB1 and HB2 are similar. Therefore, the double pulse test for the IGBT modules can be done at the half-bridge HB1 like in the Figure 6.7. The setup is similar to SiC MOSFET double pulse test with some major modifications:

- Lower DC link capacitor C3, C4 and the half-bridge HB2, HB3 are removed
- The load inductor is connected directly to the AC terminal of the HB1
- DC- terminal is connected directly to the neutral terminal

- The decoupling capacitor Cr is installed across HB1 directly at its DC+, DC- terminals

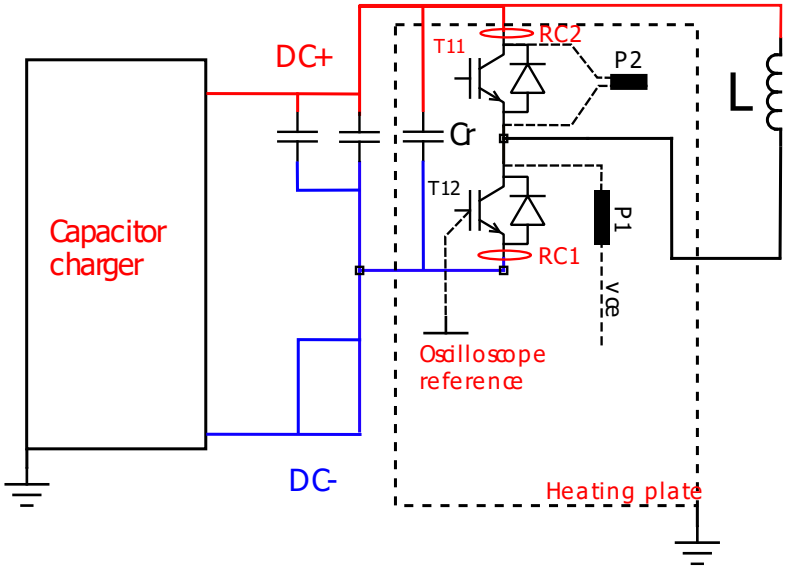


Figure 6.7: *IGBT's double pulse test setup.*

The oscilloscope reference is referred to the Kelvin terminal of T12, the voltage across T12 is measured with the 1:100 passive probe. The voltage across T11 is measured with the voltage differential probe. The Rogowski coils RC1, RC2 are used to measure the current going through T12, T11 correspondently.

The worst-case scenario for the IGBT switching is defined at V_{DC} = 900V, IL = 600A, T_j = 25°C. The targets of the characterization of the IGBT is different from the SiC MOSFET, which focus more on the optimization of the total transition time than the switching losses. To have shorter transition times, the switching speed should be faster. To protect the IGBT from the overvoltage at high switching speed, the decoupling capacitors 450nF Cr are implemented in parallel with the half-bridge HB1, HB2 (Figure 6.7) to reduce the commutation loop's inductance from 48nH to 28nH. The active clamping is also used.

6.2.2 IGBT turn-off characterization

To reduce the design time and effort, the IGBT gate drivers use the same gate driver of SiC MOSFET with -5V turn-off gate voltage. There is an additional Cgoff circuit with C_{goff} = 100nF, RC = 200Ω in parallel with the gate turn-off resistor like in the Figure 6.8, which is described in Chapter 4.5.2. The capacitor C_{goff} will flash out the gate charge at the beginning of

the turn-off process which will significantly reduce the miller plateau and the total turn-off delay time (Figure 6.9).

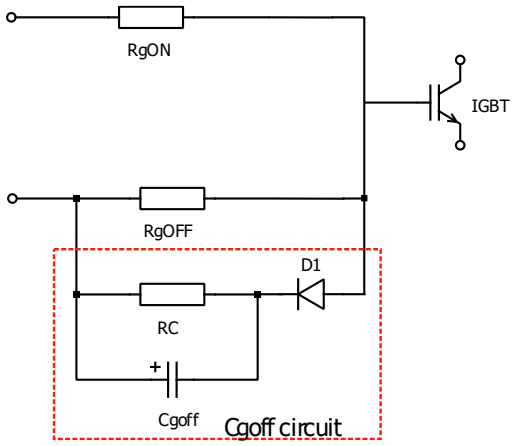


Figure 6.8: *C_{goff} circuit to reduce the turn-off delay time.*

The measurement result in the Table 6.2 shows that the optimal R_{goff} is at 4.5Ω with the total turn-off transition time is 1052ns.

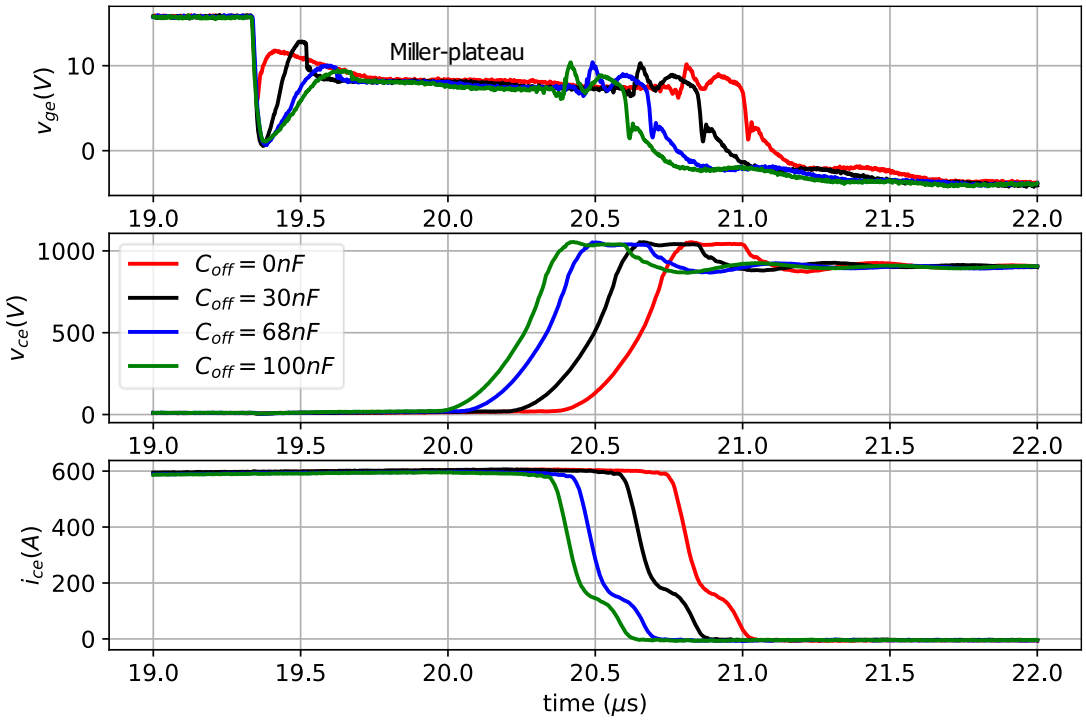


Figure 6.9: *C_{goff} circuit switching waveform with different C_{goff}. Switching conditions: V_{DC} = 900V, IL = 600A, T_j = 25°C, RC = 200Ω, R_{goff}=7.5Ω, V_{gsoff} = -5V, TVS's breakdown voltage at 1020V.*

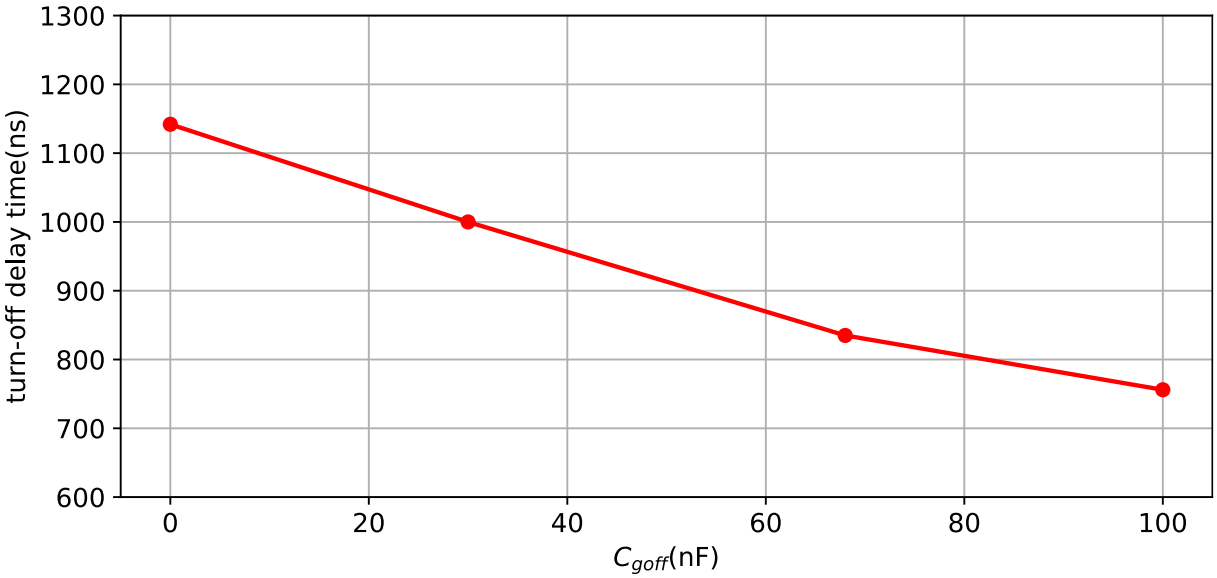


Figure 6.10: *Turn-off delay time with different C_{goff}. Switching conditions: V_{DC} = 900V, IL = 600A, T_j = 25°C, RC = 200Ω, R_{goff}=7.5Ω, V_{gsoff} = -5V.*

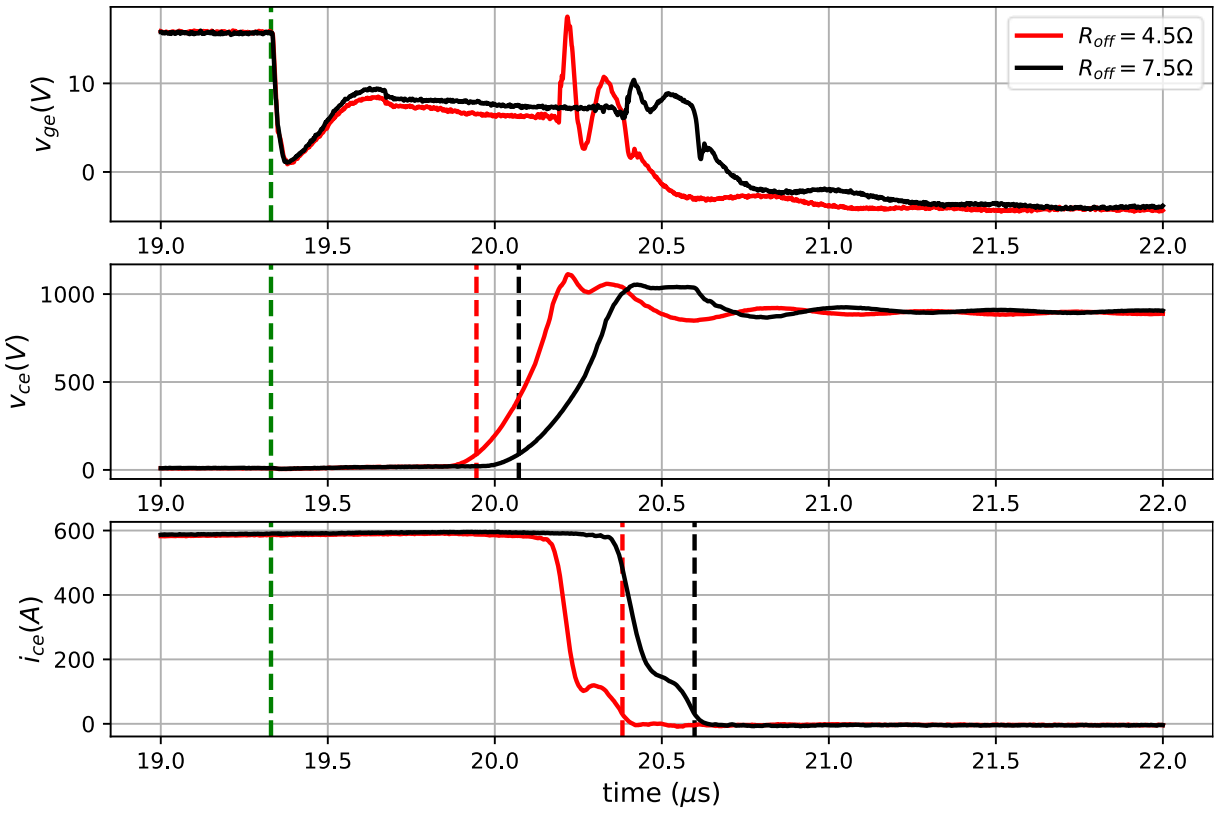


Figure 6.11: *C_{goff} circuit with different R_{goff} = 4.5Ω, 7.5Ω . The green dashed line marks the start of the transition, the dashed lines mark the end of the turn-off delay phase and the dash-doted lines mark the end of the transient phase. V_{DC} = 900V, IL = 600A, T_j = 25°C.*

Table 6.2: *Turn-off delay and transient phases of different R_{goff}.*

R_{goff} (Ω)	Delay phase (ns)	Transient phase(ns)	Peak voltage(V) @T_j = 25°C
4.5	615	437	1116
7.5	741	527	1065

The turn-off losses of the IGBT is also measured at the nominal operating condition: V_{DC} = 750V, T_j = 25°C, 125°C, 150°C.

The turn-off losses get higher at higher temperature due to the slower du/dt and the tail current (Figure 6.13). According to Bryant *et al* [79] the du/dt's temperature dependence is because the ratio $C_O / (g_m \tau_G)$ increase with the temperature. With C_O is the charge extraction capacitance, the transconductance g_m, and the gate discharging time constant $\tau_G = R_G \cdot C_{GC}$.

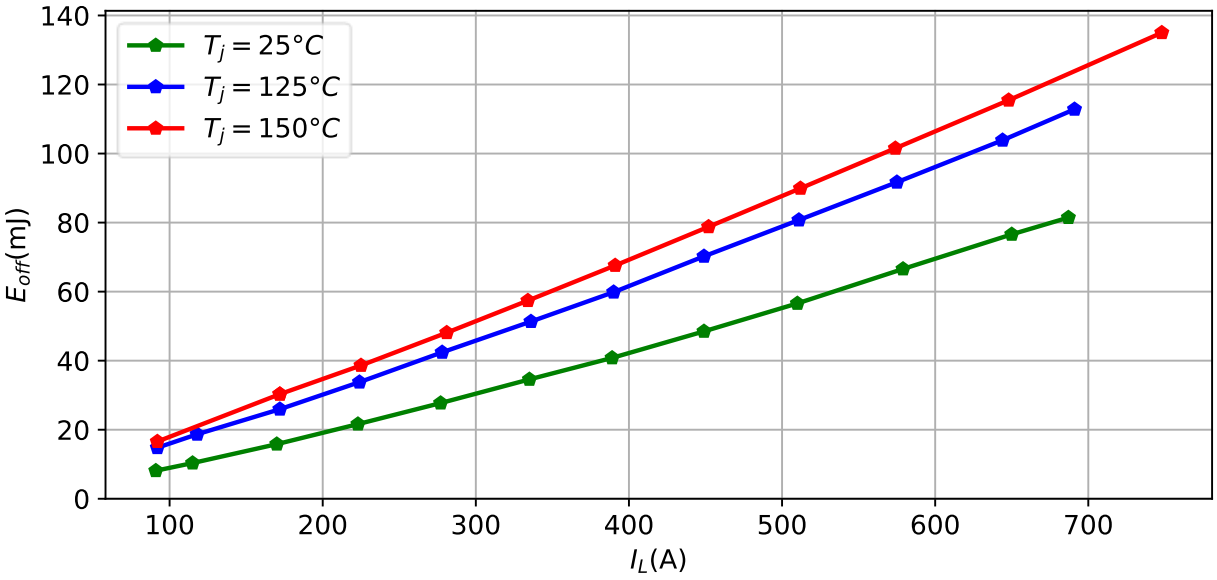


Figure 6.12: *Turn-off losses at different load currents and temperatures. Switching conditions: TVS breakdown voltage at 1020V,* V_{DC} *=750V,* R_{goff} *= 4.5Ω,* C_{goff} *= 100nF, RC = 200Ω,* V_{gsoff} *= -5V.*

The IGBT's turn-off voltages and currents at different junction temperature can be seen in Figure 6.13. Active clamping is used to protect the device from overvoltage.

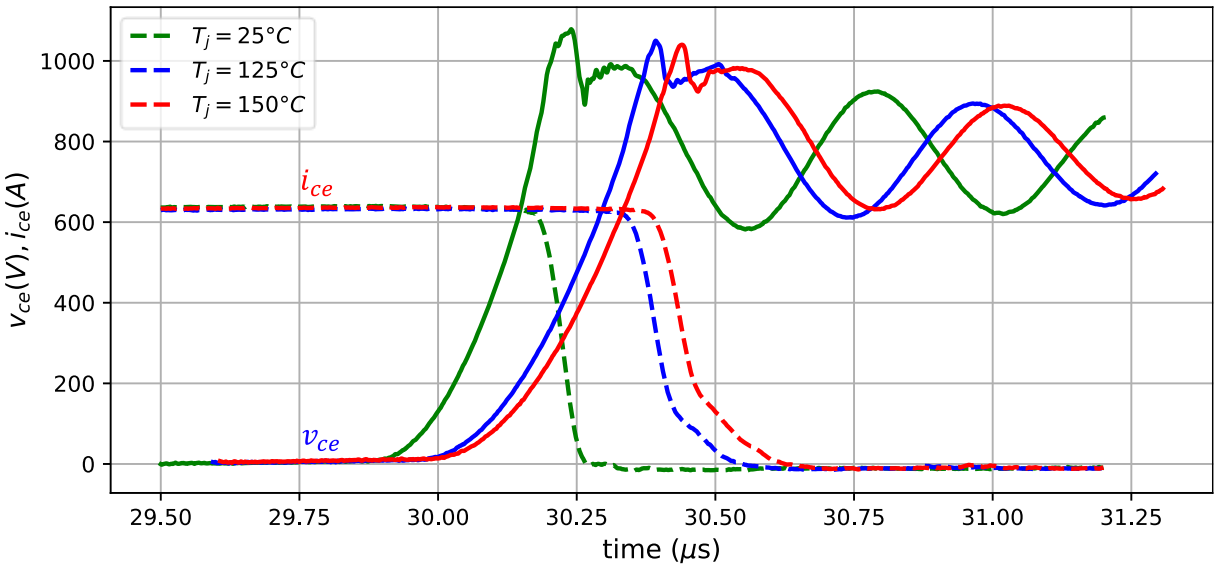


Figure 6.13: *Turn-off transients at different junction temperature. Switching conditions: TVS breakdown voltage at 1020V,* V_{DC} *=750V, IL = 600A,* R_{goff} *= 4.5Ω,* C_{goff} *= 100nF, RC = 200Ω,* V_{gsoff} *= -5V.*

6.2.3 IGBT turn-on characterization

To find the optimal R_{gon}, the double pulse test was done with different R_{gon} at V_{DC} = 900V, IL =600A, T_j = 25°C. Because of the low commutation loop inductance, it is possible to reduce the R_{gon} to zero Ω. However, the high turn-on current peak at high temperature is out of the SOA of the IGBT. At T_j = 150°C, the peak current can reach 1260 A which is out of the limit of the IGBT at 1200A [69] (Figure 6.14). To limit the turn-on peak current below the SOA, R_{gon} = 2.2Ω was chosen. The total transition time at turn-on IGBT is 485ns (Table 6.3).

Table 6.3: *Turn-on delay and transient phases of different* R_{gon}.

R_{gon} (Ω)	Delay phase (ns)	Transient phase(ns)	Peak current(A) @T_j = 150°C
0	112	168	1260
2.2	155	330	1020

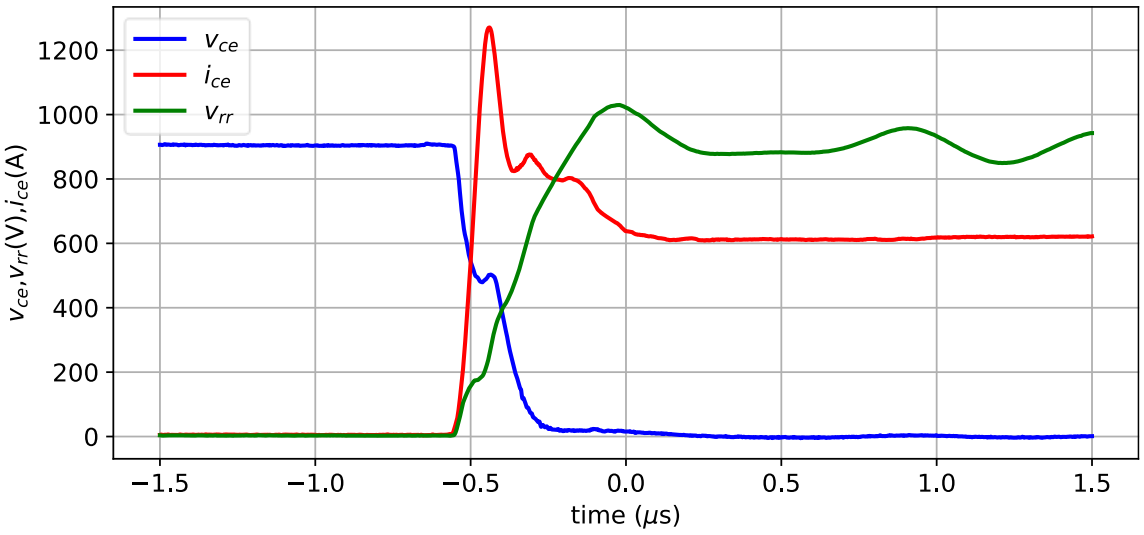


Figure 6.14: *IGBT's turn-on switching waveforms with R_{gon} = 0Ω,* V_{DC} *= 900V, IL = 600A, T_j = 150°C.*

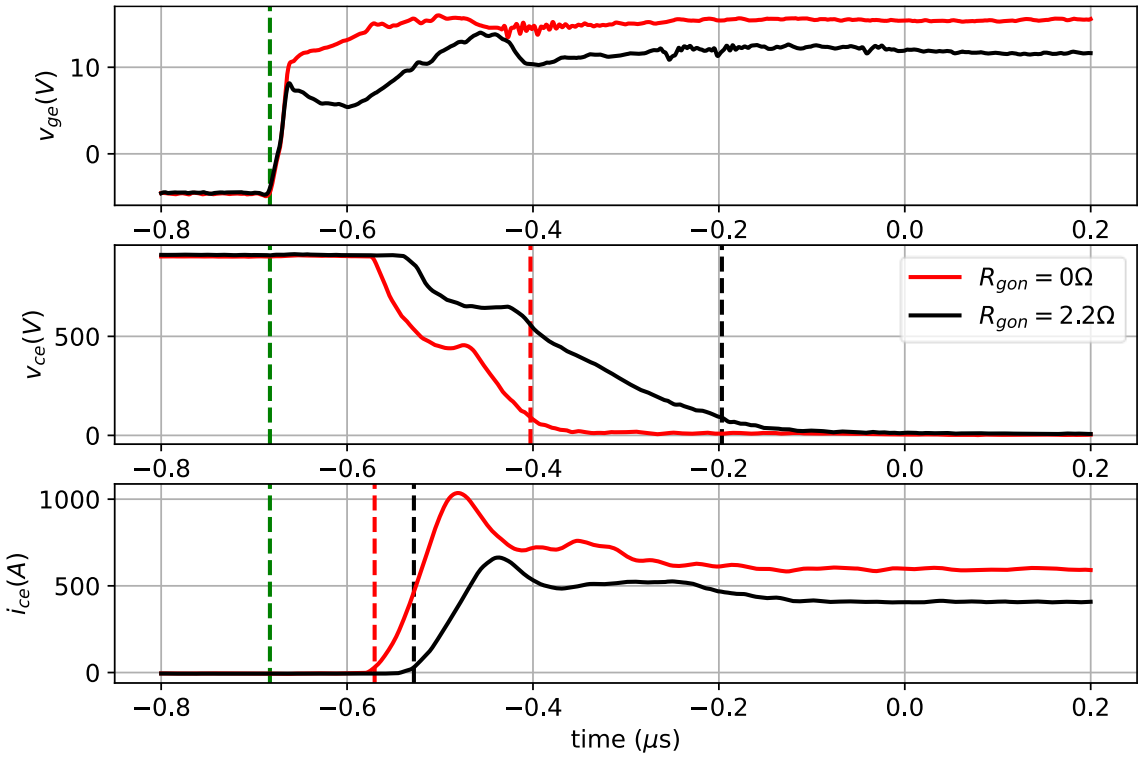


Figure 6.15: *Turn-on switching waveforms with different R_{gon} = 0Ω, 2.2Ω .The green dashed line marks the start of the transition, the red and black dashed lines mark the end of the turn-on delay phase and the dash-doted red and black lines mark the end of the transient phase.* V_{DC} *= 900V, IL = 600A, T_j = 25°C.*

The IGBTs experience parasitic turn-on during the reverse-recovery voltage slope, attributed to their high turn-off gate voltage (-5V). The phenomenon gets worse at higher temperature because of lower threshold voltage [70]. The parasitic turn on effect can be observed on the i_{ce} waveform on the Figure 6.16. The turn-on losses and reverse-recovery losses on the diodes can be seen in the Figure 6.17 and Figure 6.18.

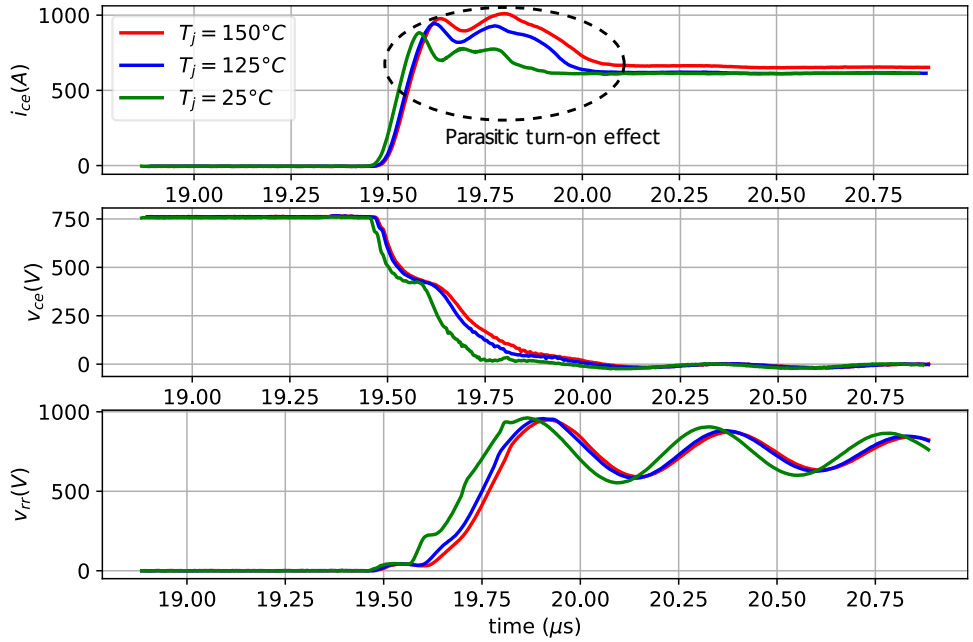


Figure 6.16: *Turn-on switching waveforms at different temperature. Switching conditions:* V_{DC} *=750V, IL = 600A,* R_{gon} *= 2.2Ω,* V_{gsoff} *= -5V.*

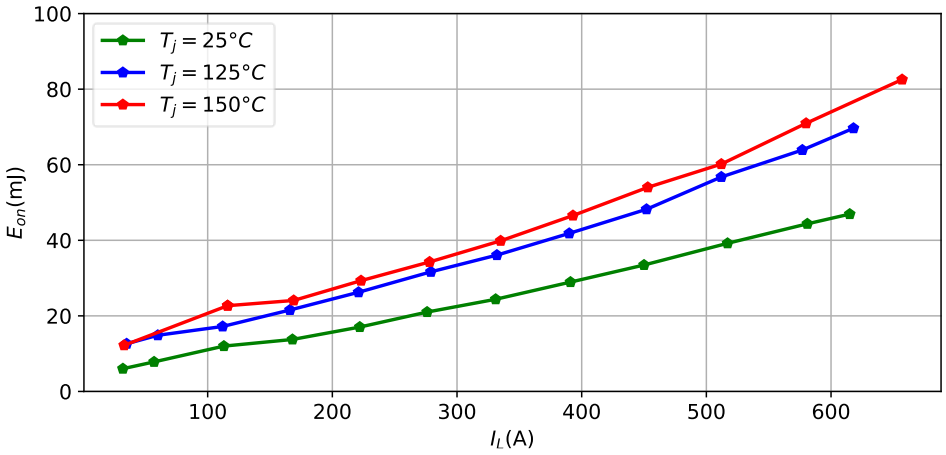


Figure 6.17: *Turn-on losses at different load current and temperature. Switching conditions:* V_{DC} *=750V,* R_{gon} *= 2.2Ω,* V_{gsoff} *= -5V.*

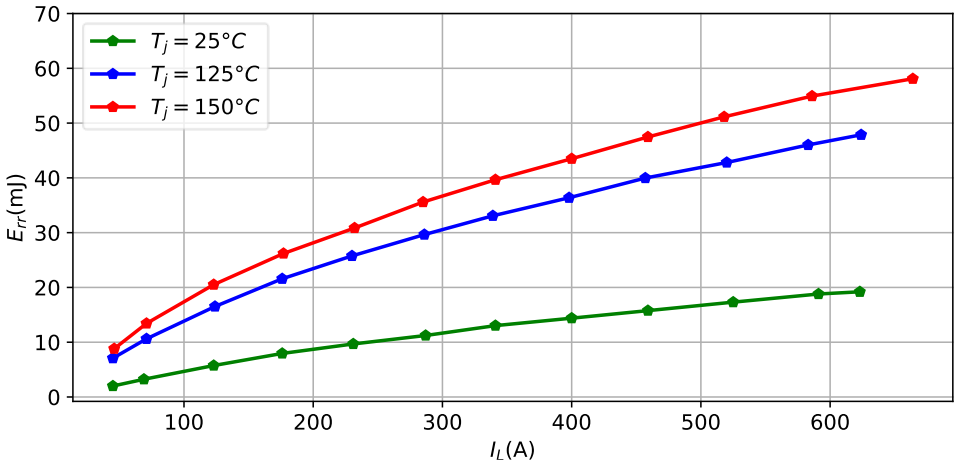


Figure 6.18: *Reverse-recovery losses at different load current and temperature. Switching conditions:* V_{DC} *=750V,* R_{gon} *= 2.2Ω,* V_{gsoff} *= -5V.*

6.3 Estimated devices' losses

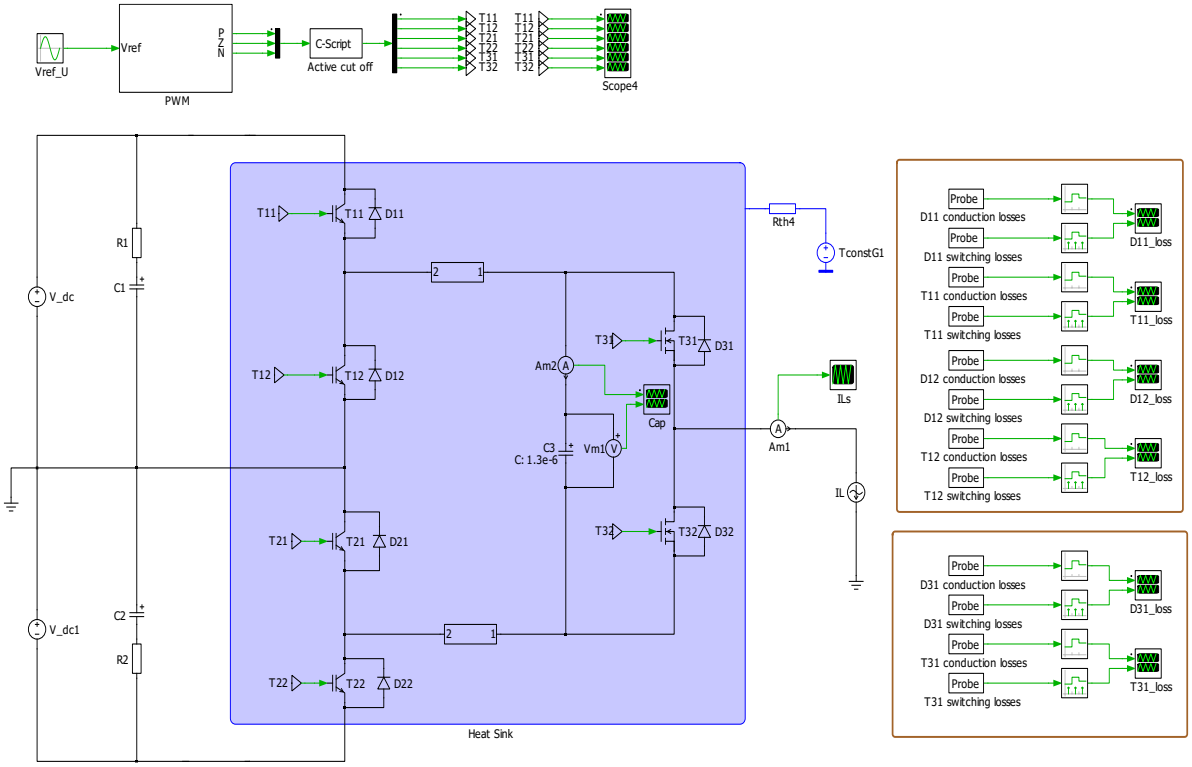


Figure 6.19: *PLECS simulation for semiconductor devices' losses estimation.*

To assess operational losses in the devices, both switching losses and conduction losses of all components are imported into the PLECS simulation. The same switching scheme is

implemented within the simulation and measure the average switching and conduction losses. It's important to note that PLECS lacks of features for modeling turn-on and turn-off delays as well as transient times. Therefore, the switching timings must be manually adjusted to closely approximate real-world switching events.

It's worth mentioning that PLECS simulations are not specifically designed for accurate transient simulations of IGBTs and MOSFET, making it challenging to precisely match the voltage and current waveforms of decoupling capacitors with real-world measurements. The switching timings and stray components within the commutation loop are fine-tuned to align with the measurement waveforms depicted in Figure 6.20 and Figure 6.21.

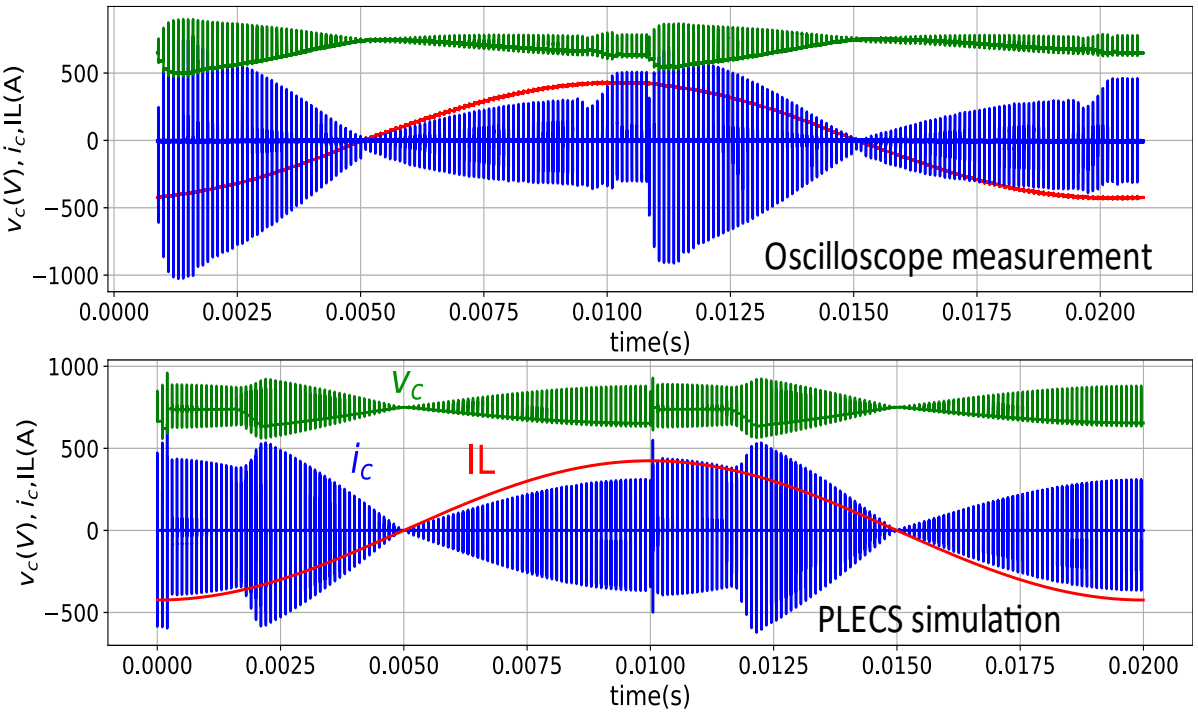


Figure 6.20: *Matching the decoupling capacitor voltage and current waveforms in PLECS simulation and real measurement.*

The reference voltage is set to 1 during the simulation, the switching frequency is at 10kHz. It's assumed that the losses in the upper-side components are equivalent to those in the lower-side components. The losses of these components are presented in Figure 6.22. To ascertain the component losses at various switching frequencies, a fixed load current of 300Arms is maintained. The outcomes of this analysis are illustrated in Figure 6.23.

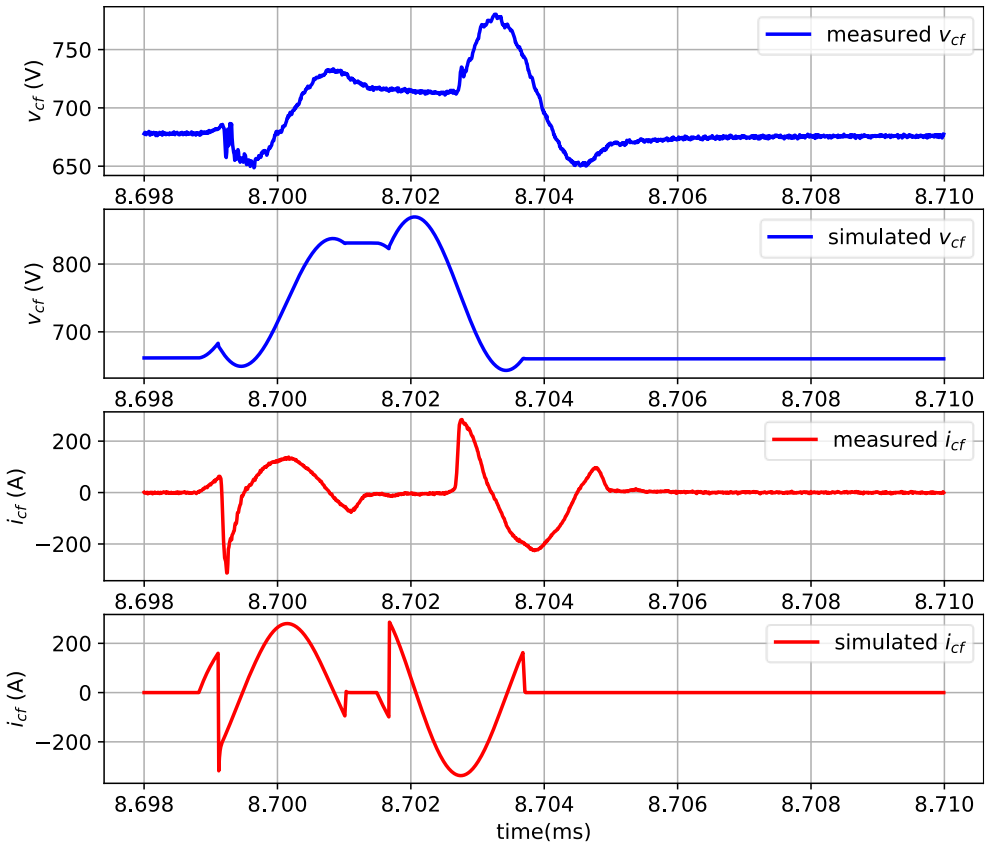


Figure 6.21: *Comparison of C_f voltage and current in real measurement and simulation.*

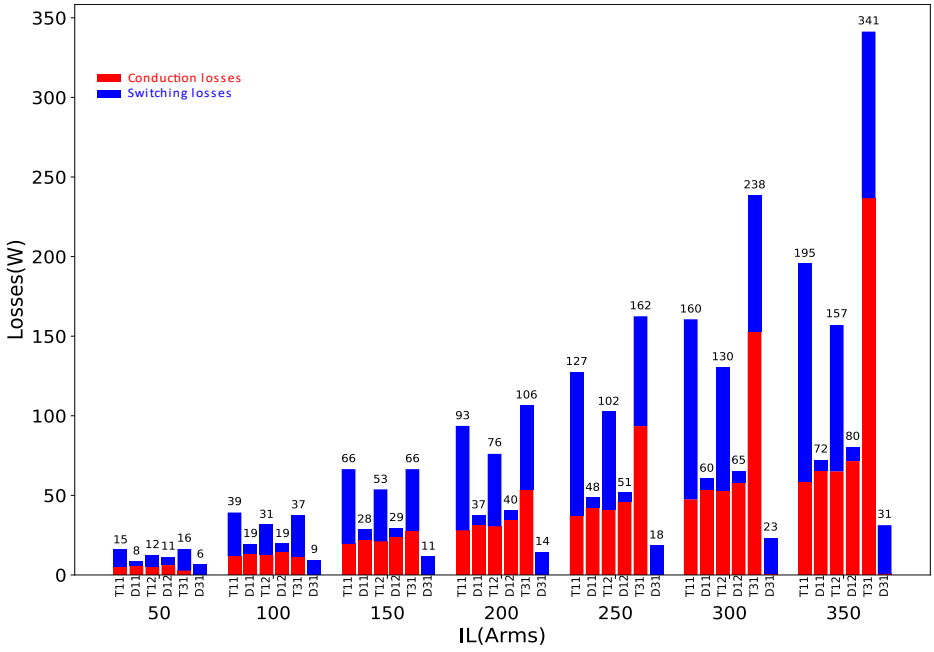


Figure 6.22: *The losses on the semiconductor devices at different operating current and* $10kHz$ *switching frequency*

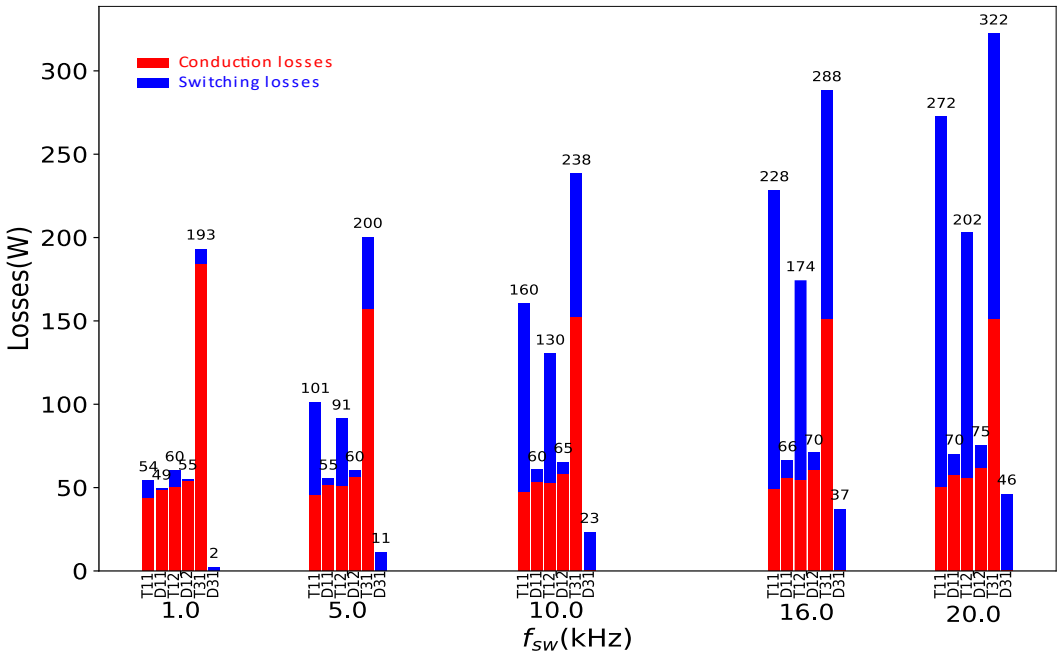


Figure 6.23: *The losses on the semiconductor at different switching frequencies with the active cut off scheme. IL = 300Arms.*

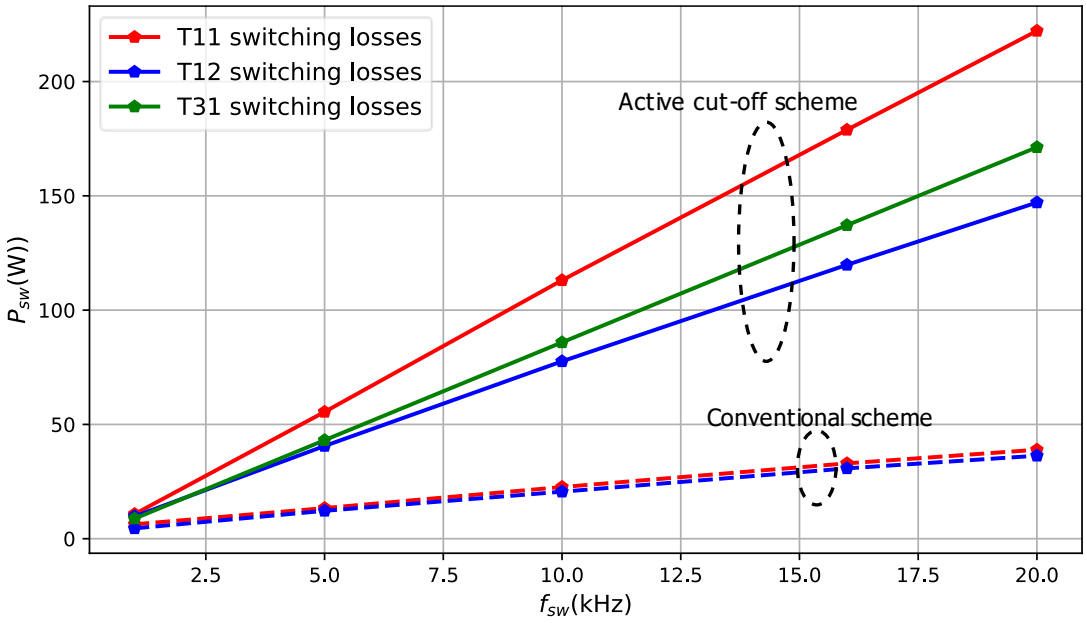


Figure 6.24: *Compare switching losses on the IGBT and MOSFET with active cut-off switching scheme (solid lines) and conventional switching scheme (dashed lines). IL = 300Arms.*

Compare to the conventional switching scheme, the active cut-off switching scheme shows significant high switching losses especially at high switching frequency (Figure 6.24).

This is the trade-off between clean switching and switching losses. It should be noticed that the IGBTs' switching losses in PLECS simulation are larger than their real switching losses.

6.4 Experimental Result

6.4.1 Three phases current waveform

In order to examine the output current waveform, the ANPC is linked to the 480µH start connected load inductor, as depicted in Figure 6.25. To mitigate the impact of high du/dt on current measurements, the phase currents (i_u, i_v, i_w) are placed after the load inductor. Furthermore, the current flowing through the filter capacitor (i_c) is also subjected to measurement. The inverter was run in 500ms until it reaches the steady state at nominal current 340Arm, the three-phase current waveform can be seen in the Figure 6.28.

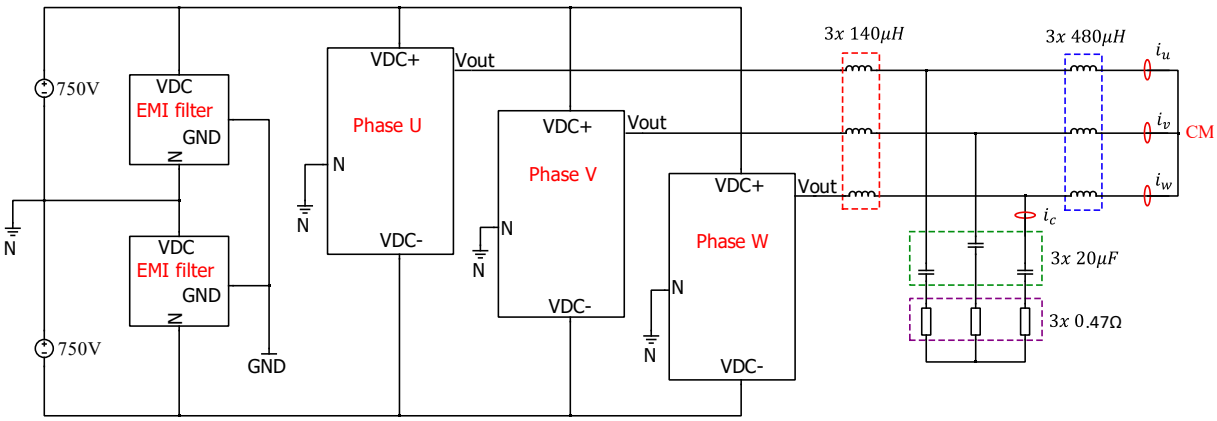


Figure 6.25: *Three phase current waveform measurement diagram.*

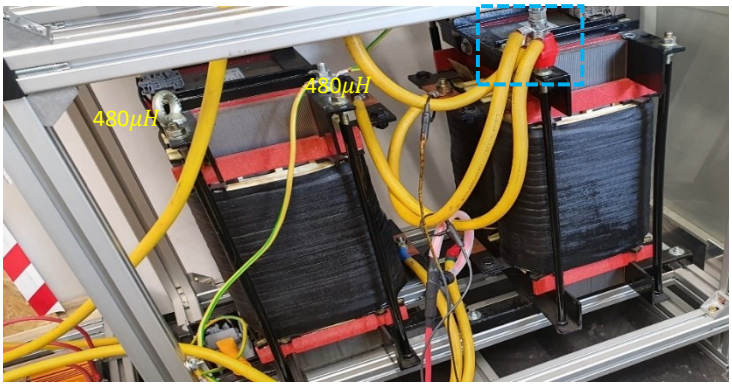


Figure 6.26: *Three phase start connected load inductors 3x 480µH-600Arms and the start point CM where the 3 phase load currents are measured.*

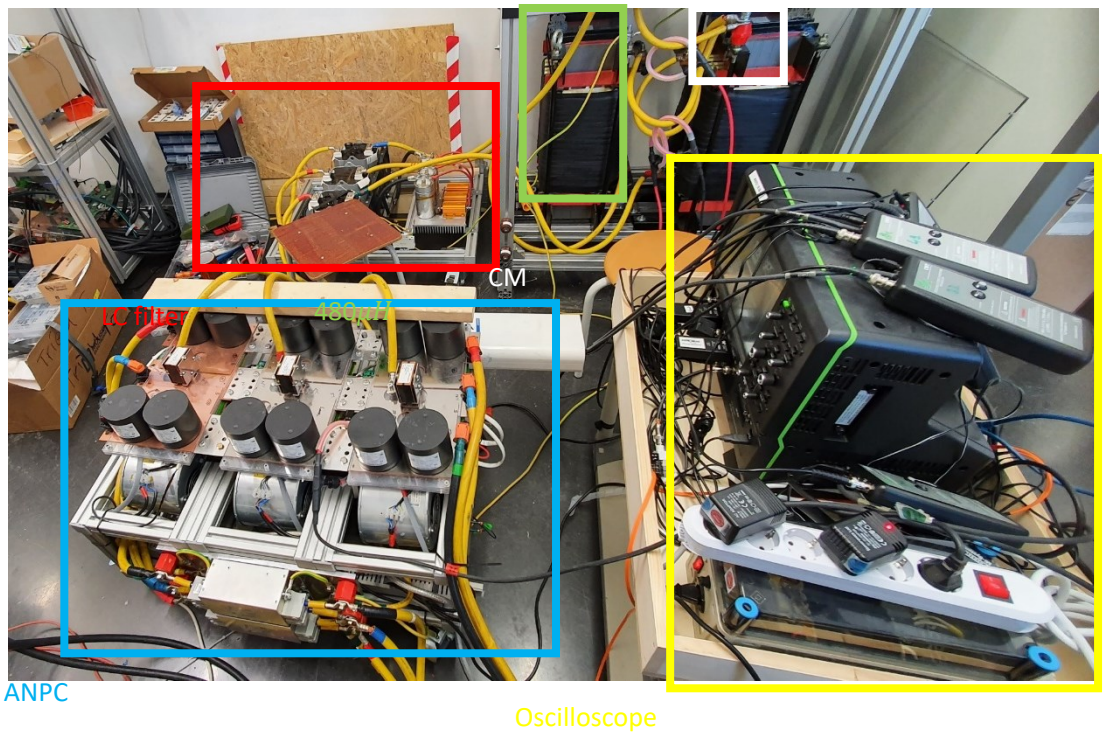


Figure 6.27: *Three phase current waveform measurement test setup.*

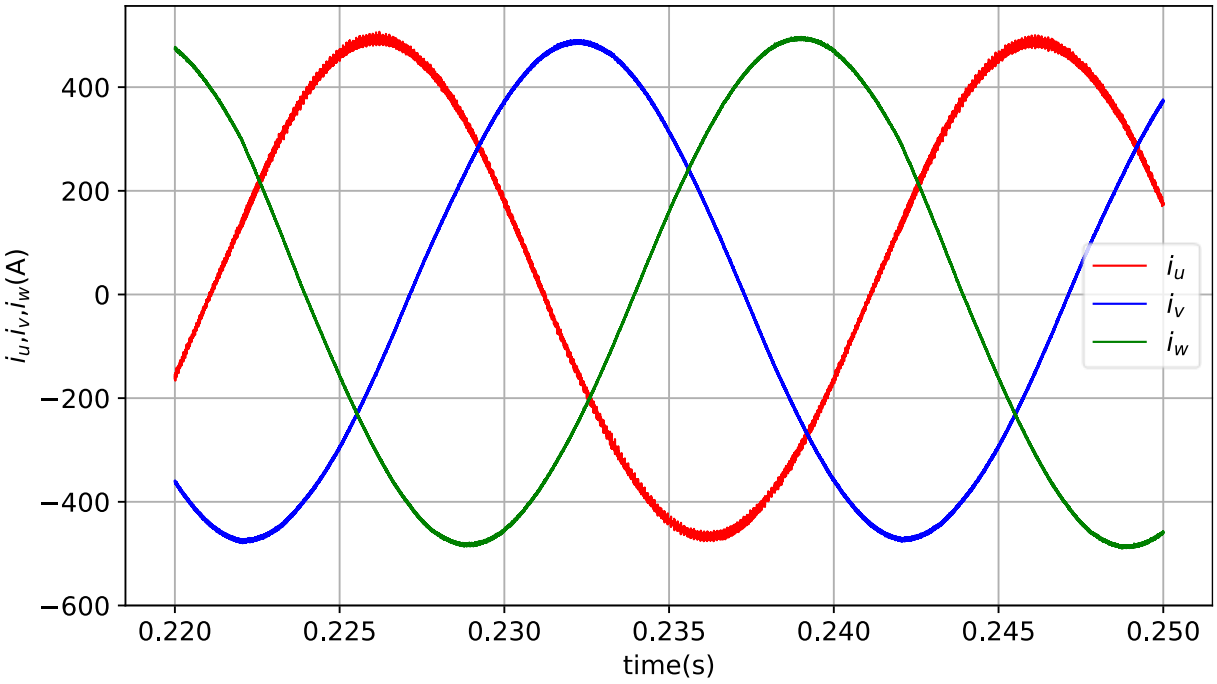


Figure 6.28: *Three phase load current waveform at the steady state nominal current 340Arms.*

The effect of the LC filter can be seen in Figure 6.29. The current ripple is completely filtered out. The high frequency current is absorbed by the filter capacitor, which is shown in Figure 6.30.

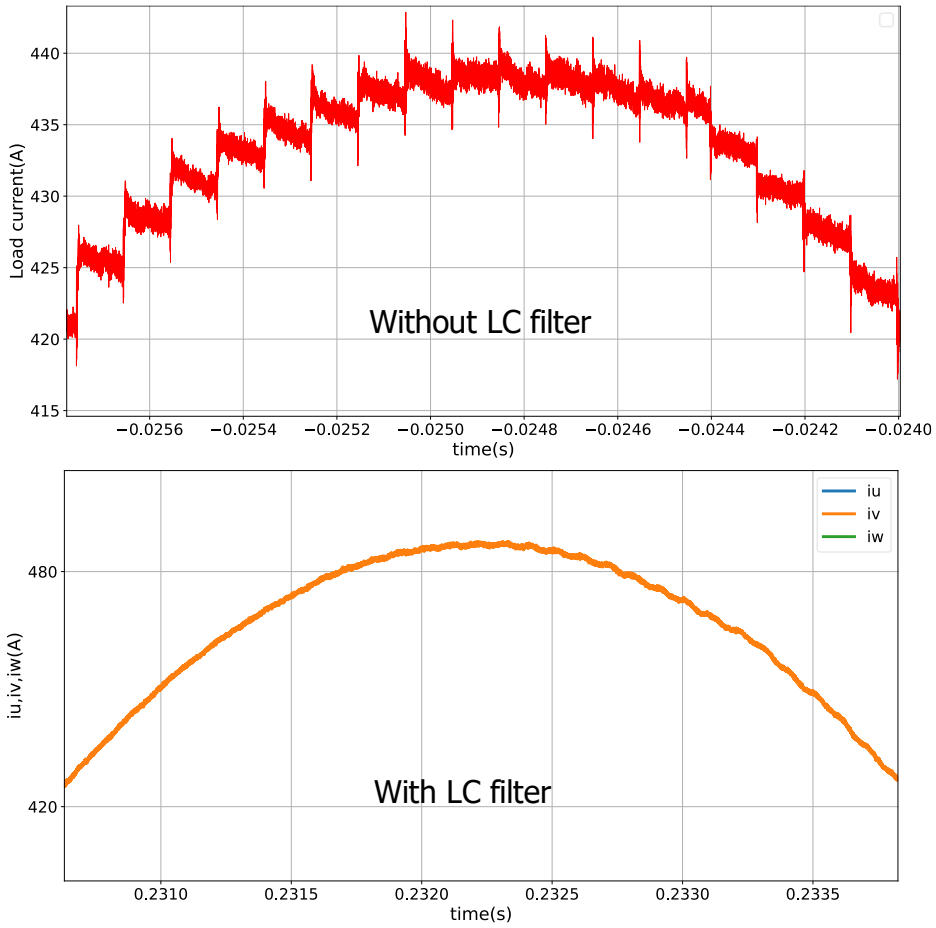


Figure 6.29: *Compare load current with and without LC filter.*

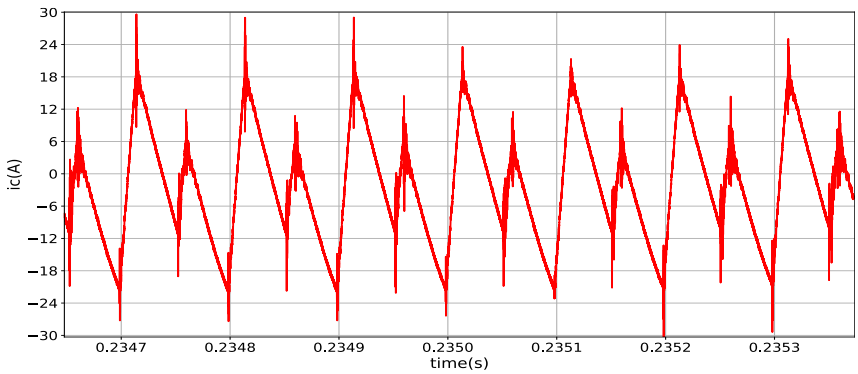


Figure 6.30: *LC filter's capacitor current:* $I_c = 8Arms$*, peak-peak current ripple = 36A.*

6.4.2 Continuous operation experiment

To monitor the temperature of critical components, the ANPC setup was configured in a single phase, as illustrated in the Figure 6.31. This configuration was operated consistently at IL = 210, 280, 305 Arms for a duration of two hours, allowing enough time for all temperatures

to stabilize. PT100 sensors were employed to gauge the temperatures of various components, including the ferrite cores, active clamping diode, heatsink, decoupling capacitor, filter inductor, and DC link capacitor (Figure 6.32). Using a temperature logger, the data was gathered and seamlessly transmitted to the user's laptop via WIFI (Figure 6.34). The temperatures were logged at 0.25Hz sampling rate. Notably, active cooling fans were installed for the decoupling capacitor and ferrite cores as can be seen in the Figure 6.35.

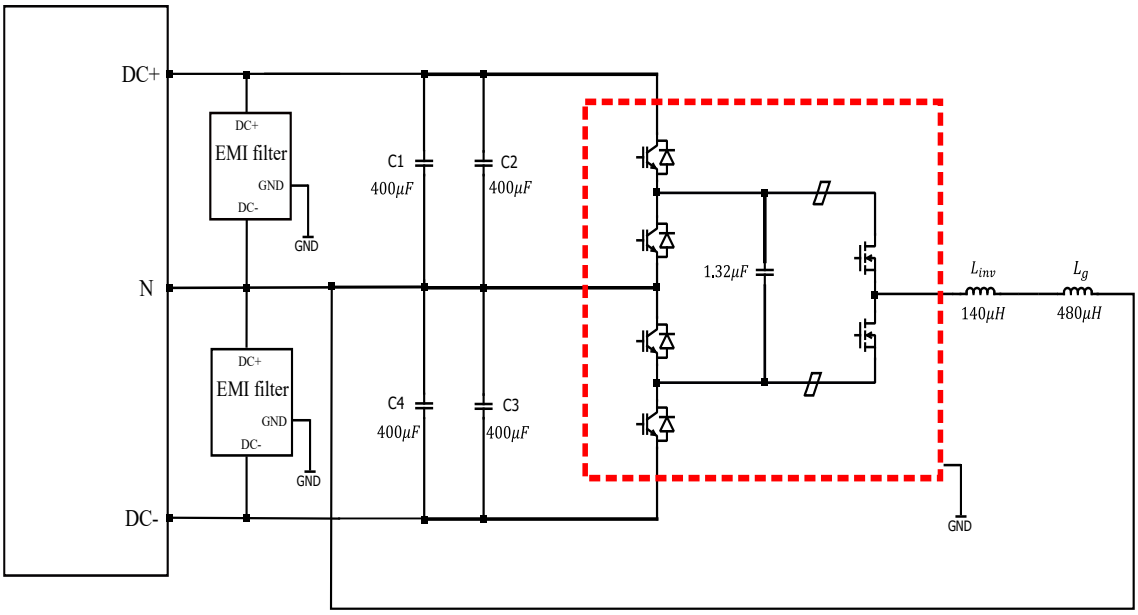


Figure 6.31: *The continuous operation experiment diagram.*

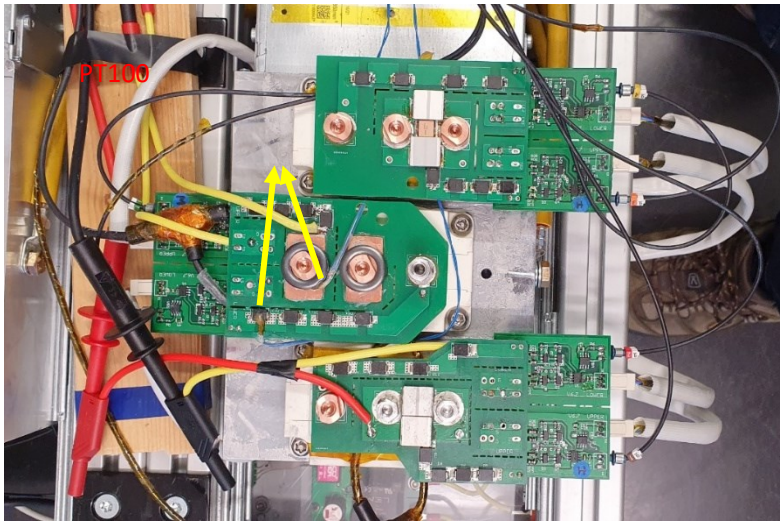


Figure 6.32: *Active clamping diode and ferrite cores temperature are measured with PT100 sensors.*

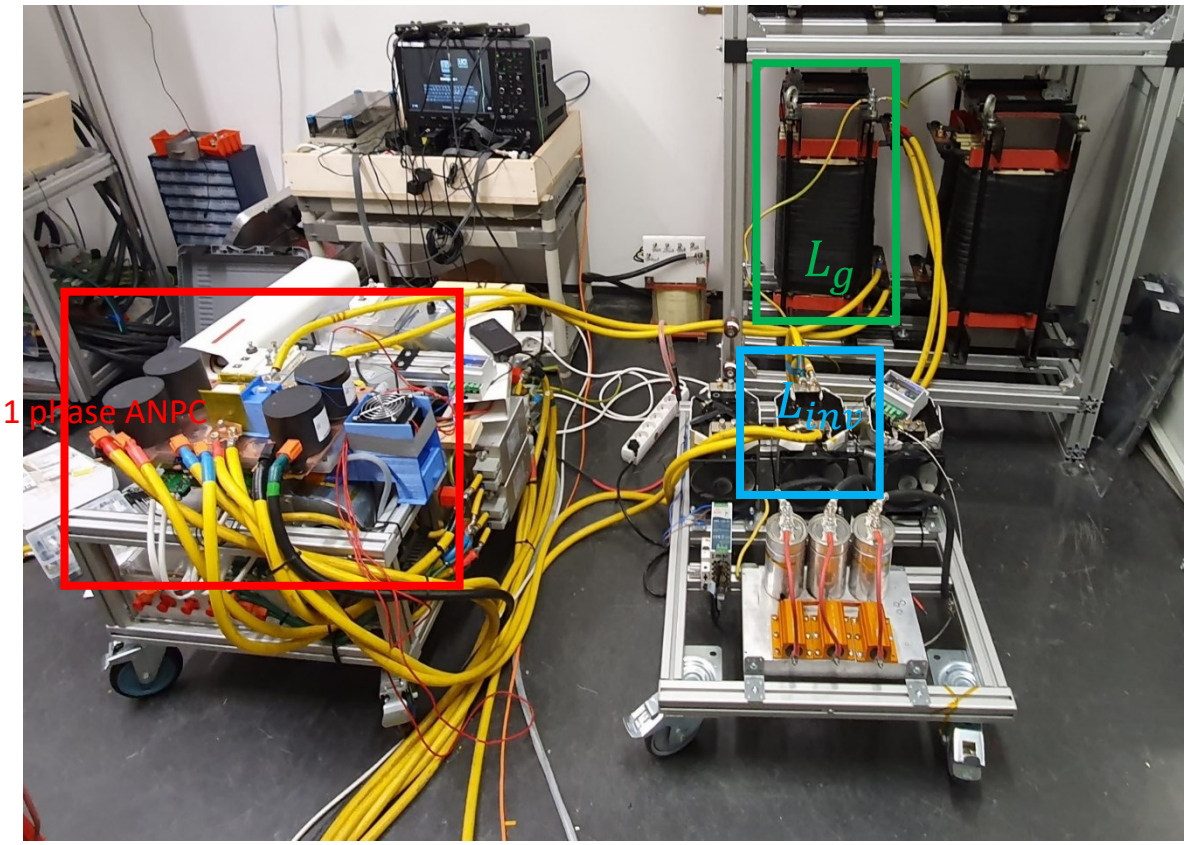


Figure 6.33: *The continuous operation experiment setup for one phase of the ANPC.*

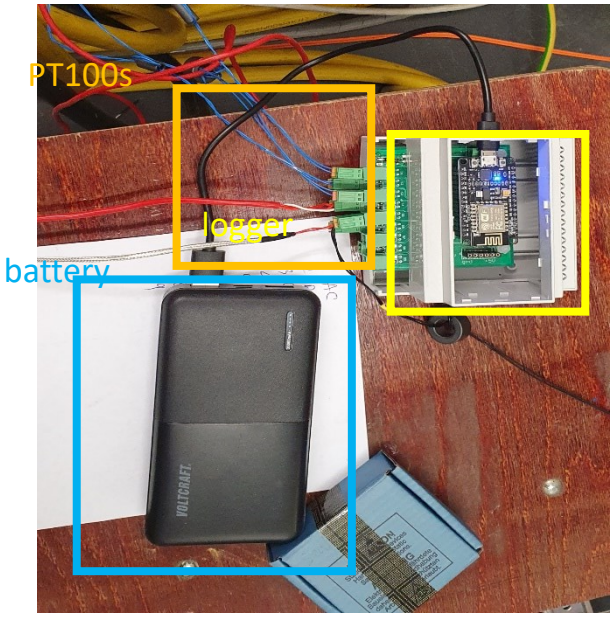


Figure 6.34: *The Wifi temperature logger device with battery supply.*

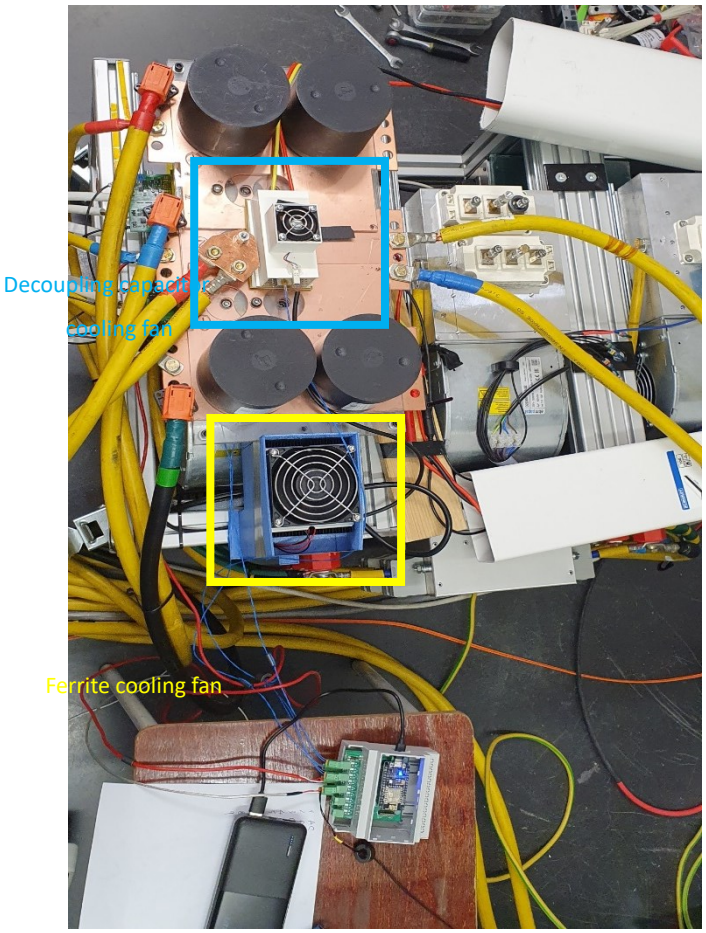


Figure 6.35: *Ferrite cores and decoupling capacitor are cooled with fans.*

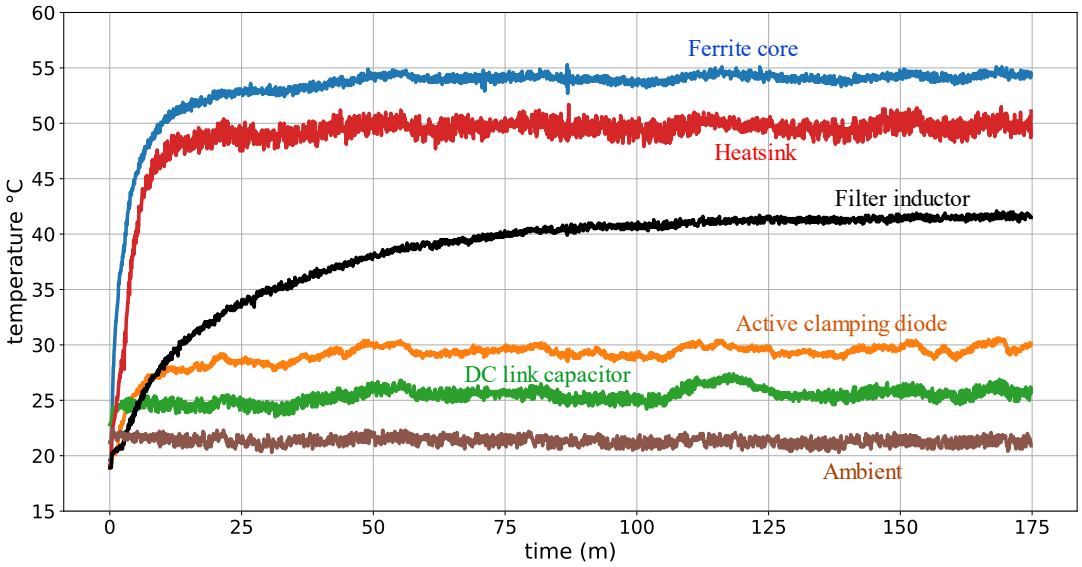


Figure 6.36: *Critical components' temperatures at IL = 210 Arms.*

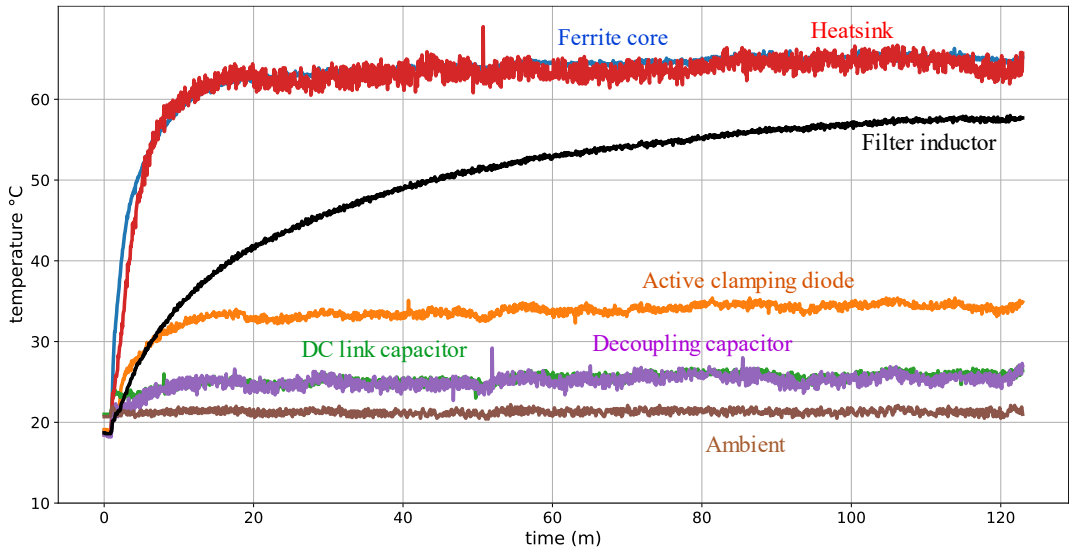


Figure 6.37: *Critical components' temperatures at IL = 280 Arms.*

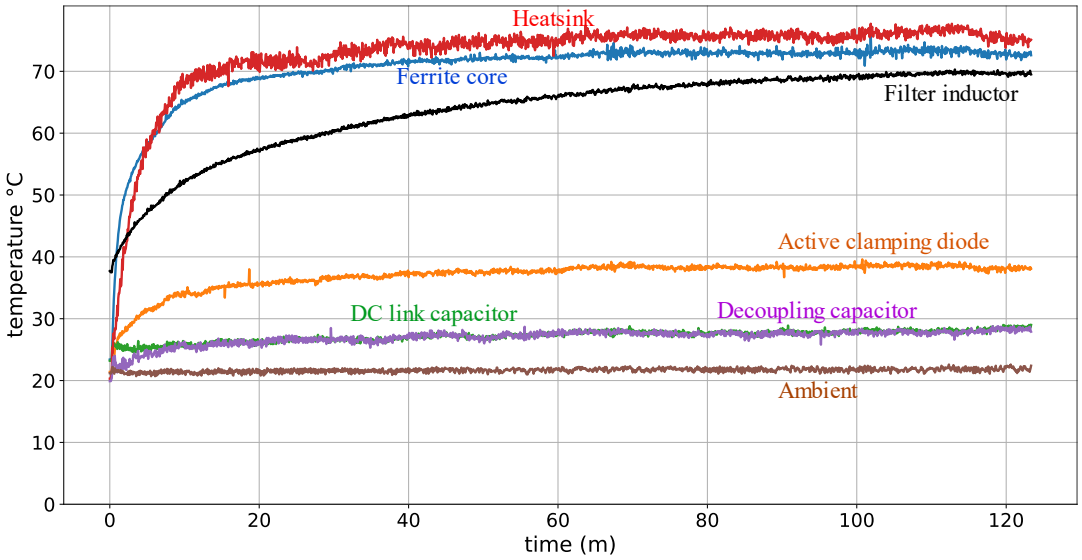


Figure 6.38: *Critical components' temperatures at IL = 305 Arms.*

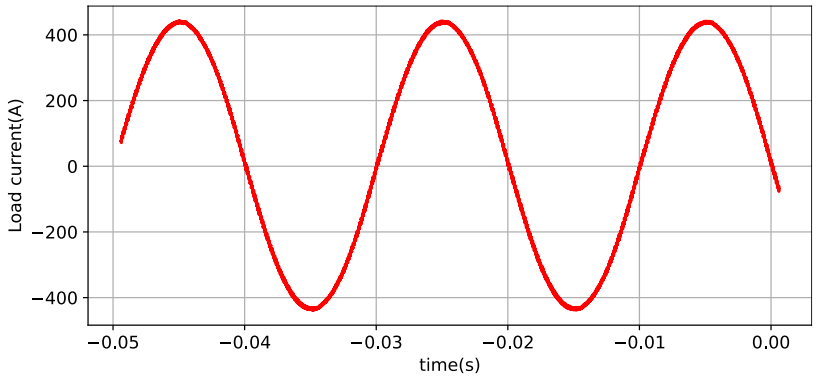


Figure 6.39: *Load current waveform at 305Arms.*

Table 6.4: *Temperatures of ANPC's critical components at different operating currents.*

	IL = 210 Arms	IL = 280 Arms	IL = 305 Arms
Heatsink	50°C	64°C	76°C
Ferrite core	54°C	65°C	73°C
Active clamping diode	30°C	34°C	38°C
DC link capacitor	26°C	26°C	28°C
Decoupling capacitor	-	25°C	28°C
Filter inductor	41°C	58°C	70°C
Ambient	21°C	21°C	22°C

6.4.3 Thermal modeling

The forced air-cooling fan of one inverter phase can be seen in the Figure 6.40, the heat sink's temperature measurement point is next to the SiC MOSFET module.

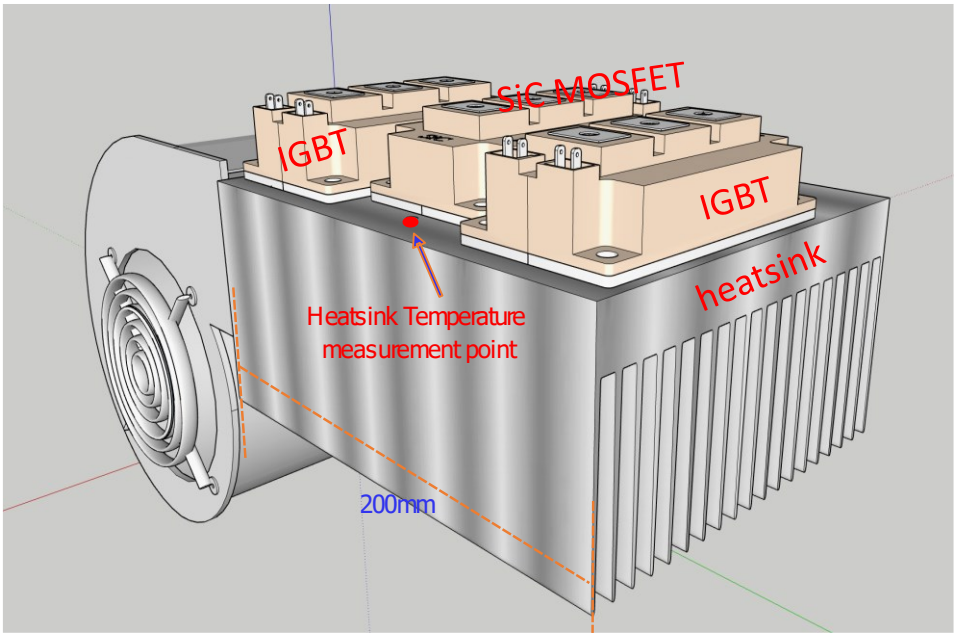


Figure 6.40: *The cooling fan and heatsink temperature measurement point.*

For simple estimation of the semiconductor switches' junction temperatures, it is assumed that the heat sink temperature underneath the SiC MOSFET, IGBT and diodes are equal to the heatsink temperature measurement point.

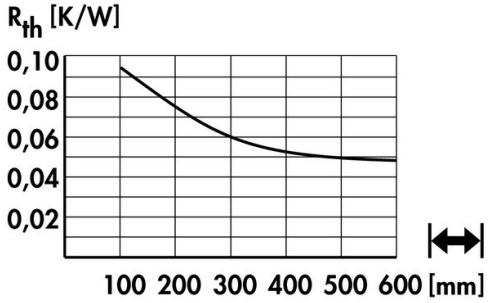


Figure 6.41: *Heatsink Fisher Elektronik LA 25 200 230, length:200mm [64].*

The steady state thermal model of one phase of the ANPC can be seen in Figure 6.42.

Table 6.5: *Thermal resistance of the ANPC's components.*

	SiC MOSFET	**TIM**	**Heatsink**	**IGBT**	**Diode**
R_{th}(K/W)	0.113	0.006	0.075	0.046	0.0929

From the steady state thermal model in Figure 6.42, the junction temperature of the semiconductor switches can be estimated as following :

The SiC MOSFET'S junction temperature:

$$T_j = P_{sic} \cdot 0.119 + T_{heatsink} \tag{6.1}$$

The IGBT's junction temperature:

$$T_j = P_{IGBT} \cdot 0.052 + T_{heatsink} \tag{6.2}$$

The diode's junction temperature:

$$T_j = P_{diode} \cdot 0.0989 + T_{heatsink} \tag{6.3}$$

The heat sink's temperature:

$$T_{heatsink} = \sum P_{loss} \cdot 0.075 + T_{ambient} \tag{6.4}$$

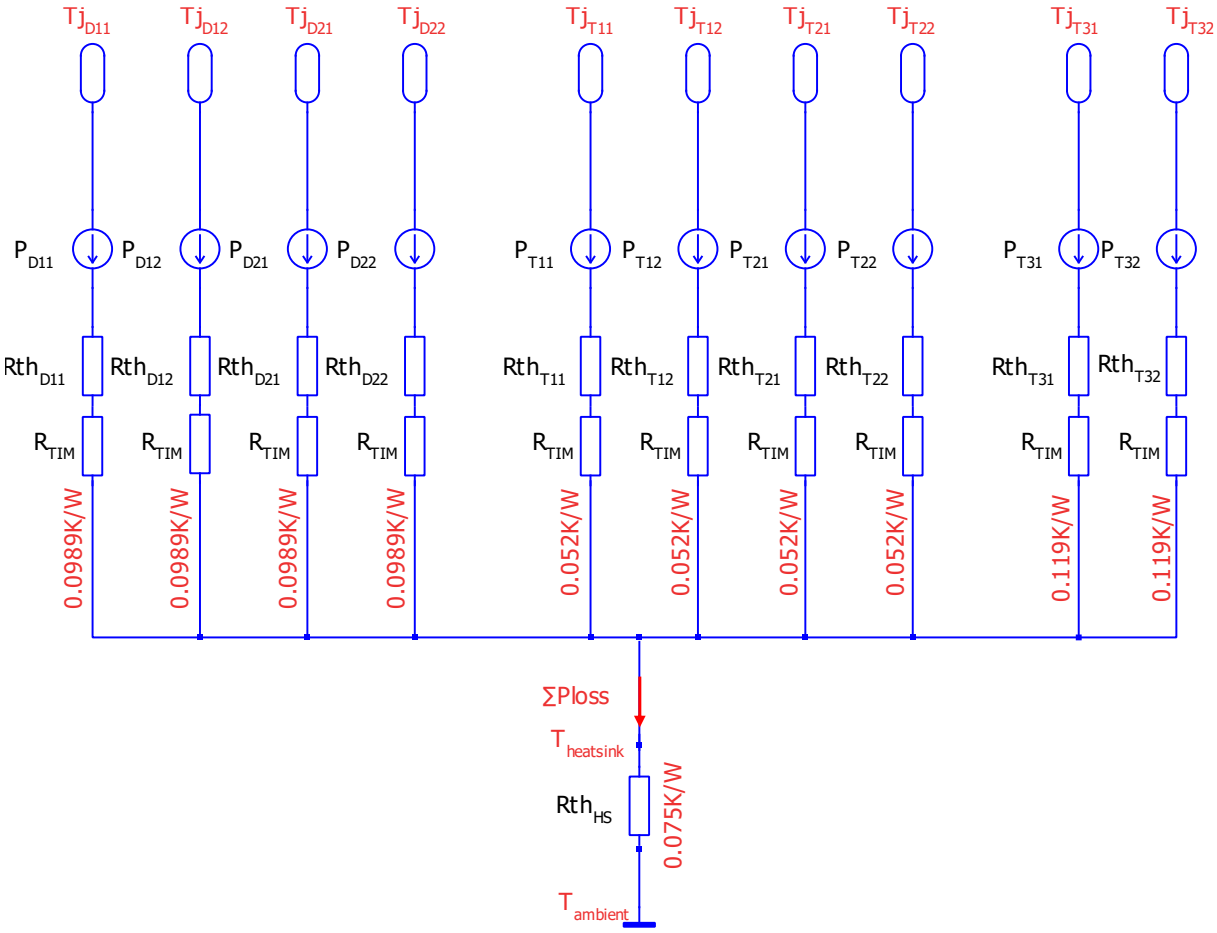


Figure 6.42: *The steady state thermal model of 2SiC hybrid ANPC.*

The PLECS simulation which has equal modulation index with the experiment setup at IL = 305 Arms is used to estimate the semiconductor switches losses and their junction temperatures are also calculated and displayed in the Table 6.6.

Table 6.6: *Estimated power losses and junction temperatures of the semiconductor devices during the continuous experiment at 22°C ambient temperature, IL = 305Arms.*

	T11	**T12**	**T21**	**T22**	**T31**	**T32**	**D11**	**D12**	**D21**	**D22**	**∑Ploss**
P(W)	92	183	183	92	228	228	14	102	102	14	1234
Tj(°C)	81	86	86	81	103	103	77	86	86	77	

If the inverter is operated at full modulation index, assumed that the ambient temperature is constant at 22°C the devices' losses and temperatures are displayed in the Table 6.7. The total loss is 1352W, the heatsink temperature is $T_{heatsink}$ = 123°C.

Table 6.7: *Estimated power losses and junction temperatures of the semiconductor devices at full modulation index and 22°C ambient temperature, IL = 305Arms.*

	T11	**T12**	**T21**	**T22**	**T31**	**T32**	**D11**	**D12**	**D21**	**D22**	**$\sum P_{loss}$**
P(W)	160	130	130	160	261	261	60	65	65	60	1352
Tj(°C)	131	130	130	131	154	154	129	129	129	129	

With the actual cooling conditions and switching losses calculation method, the relationship between the maximum output current of the inverter over the maximum switching frequency is shown in Figure 6.43. It shows that at 300Arms, the inverter's switching frequency is limited at 10kHz to avoid overheating the SiC MOSFET. When the output current increases to 350Arms, the maximum switching frequency is significantly reduced to 2kHz.

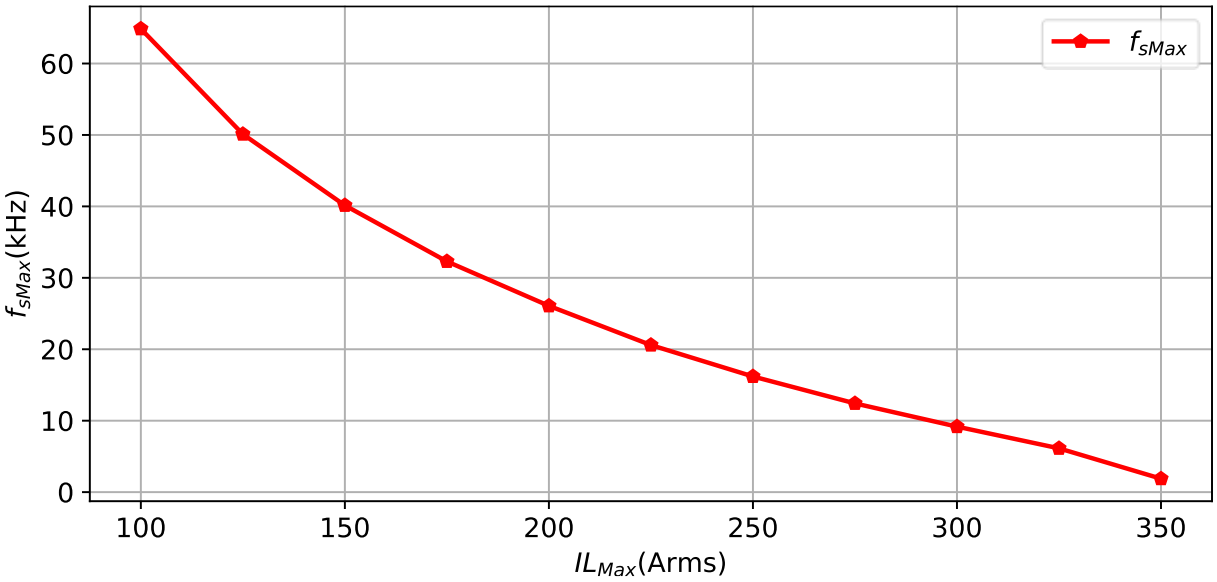


Figure 6.43: *2SiC hybrid ANPC's maximum output current and maximum switching frequency for the active cut-off switching scheme to limit the SiC MOSFET's junction temperature below 150°C.*

The inverter efficiency at the rated current when only count the losses on semiconductor devices is around 99.2%.

$$\eta = \frac{P_{out}}{3 \cdot \sum P_{loss} + P_{out}} \cdot 100\% = 99.2\% \tag{6.5}$$

6.5 Compare 2SiC and 4SiC hybrid ANPC

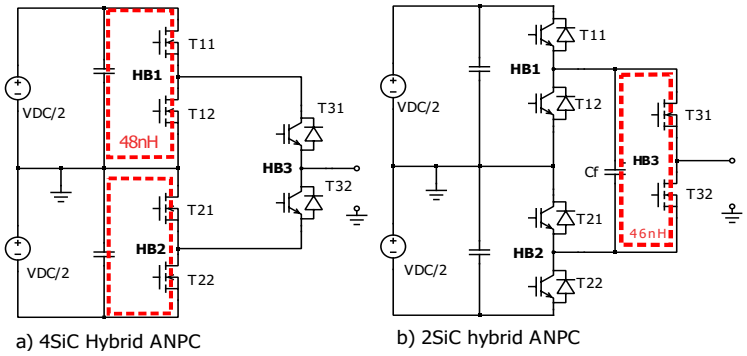


Figure 6.44: *Compare a) 4SiC hybrid ANPC and b) 2SiC hybrid ANPC.*

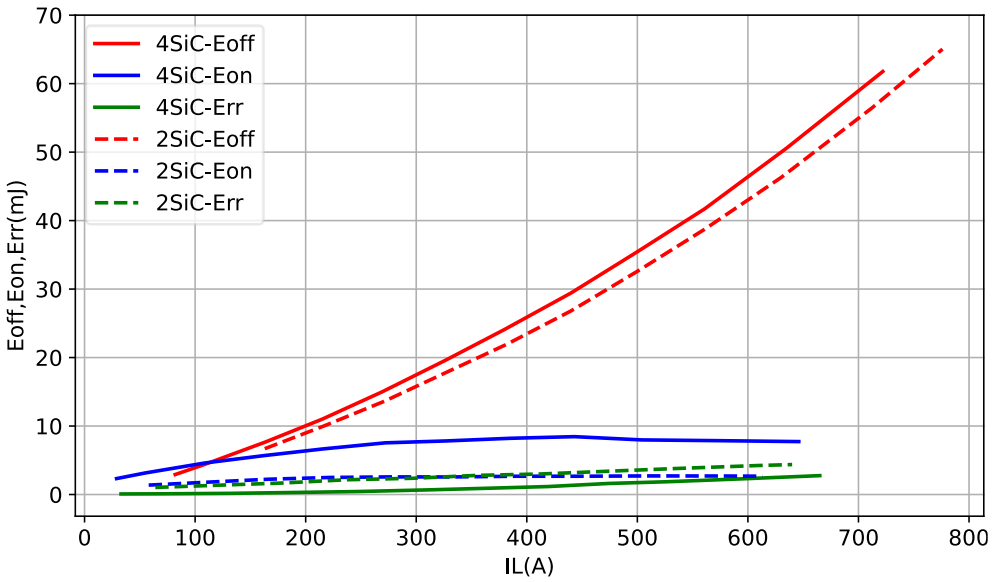


Figure 6.45: *Compare the switching energies of SiC MOSFET in 2SiC hybrid ANPC (dashed lines) and 4SiC hybrid ANPC (solid lines) at 1500V, 150°C.*

Figure 6.44 shows the commutation loops' inductances of 4SiC hybrid ANPC (Figure 6.44a) and 2SiC hybrid ANPC (Figure 6.44b). To compare the performance of the two topologies, the switching energies of SiC MOSFET in 4SiC hybrid ANPC are measured with

the gate parameters and switching conditions like Table 6.8. The turn-on, turn-off and reverse-recovery energies at 150°C junction temperatures are displayed in the Figure 6.45. Because the commutation loops' inductances and the switching conditions are quite similar, the switching energies are near together. The turn-on and reverse-recovery energies are not equal because of 2SiC ANPC uses dual ferrite cores and higher turn-off gate voltage. To make a fare comparison, both topologies are switched at 10kHz with the conventional PWM schemes: PWM-1, PWM-2 as mentioned in Chapter 1.

Table 6.8: *Switching conditions of 2SiC and 4SiC hybrid ANPC.*

	2SiC ANPC	**4SiC ANPC**
$\boldsymbol{L_\sigma(nH)}$	46	48
Active Clamping	yes	yes
Dual Ferrite cores	yes	no
V_{DC} (V)	1500	1500
PWM	PWM-2	PWM-1
Ambient Temperature (°C)	22	22
Switching frequency(kHz)	10	10
Modulation index	1	1

The ambient temperature is assumed to be stable at 22°C for both cases. The two topologies are implemented in PLECS to estimate the losses on each semiconductor switches. In 4SiC ANPC, SiC MOSFET T12's total losses are dominated for the load current above 350Arms, as depicted in Figure 6.46. While in 2SiC ANPC, SiC MOSFET T31's total losses are dominated, as shown in Figure 6.47.

In the 2SiC hybrid ANPC, the junction temperature of T31 reaches 150°C when the load current is around 320 Arms which is depicted in the Figure 6.48, while in the 4SiC hybrid ANPC, T12's junction temperature reaches 150°C when the load current is around 420Arms

which can be seen in the Figure 6.49. In this test setup condition, double SiC chip area doesn't result in double output current.

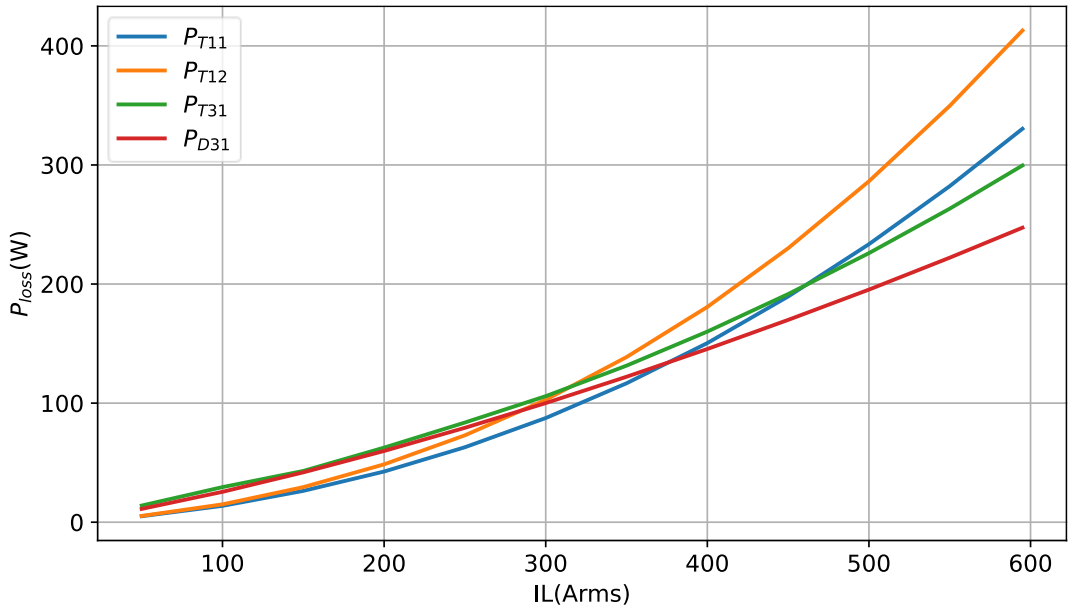


Figure 6.46: *The total losses on each semiconductor switch in 4SiC hybrid ANPC at 10kHz switching with PWM-1, modulation index = 1.*

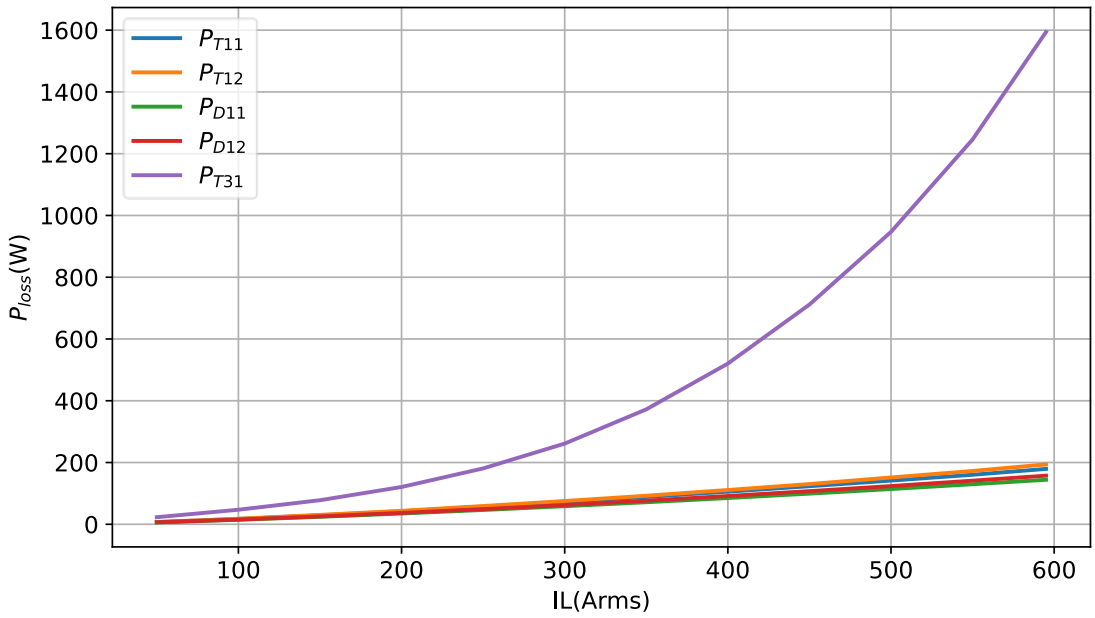


Figure 6.47: *The total losses on each semiconductor switch in 2SiC hybrid ANPC at 10kHz switching with PWM-2, modulation index = 1.*

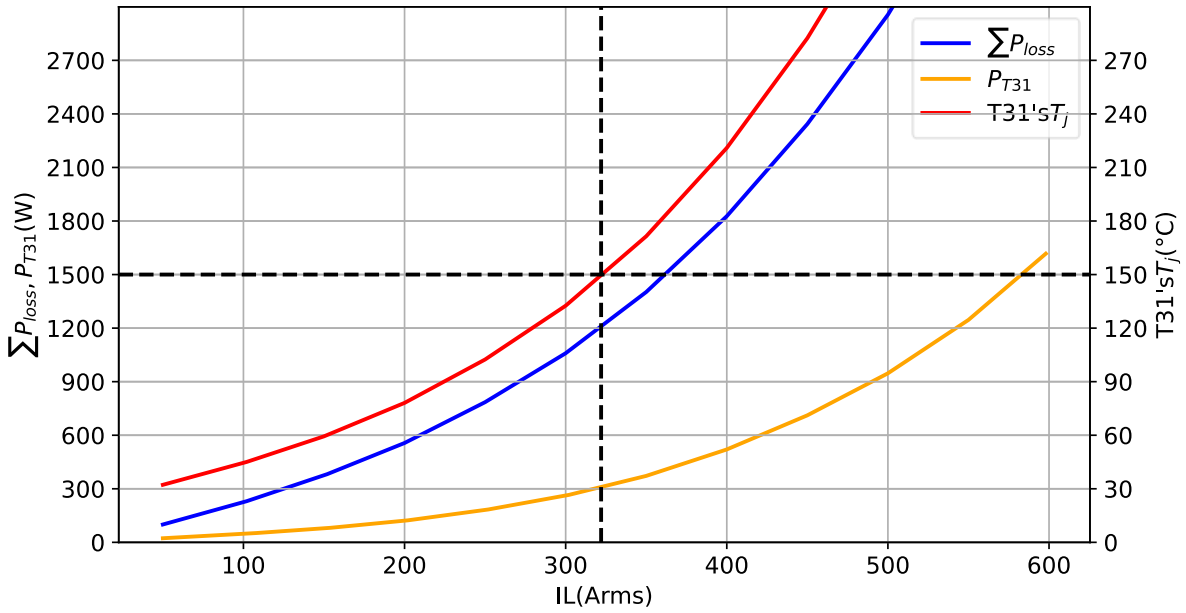


Figure 6.48: *The total losses of T31 in 2SiC hybrid ANPC at 10kHz switching frequency. The maximum load current that 2SiC ANPC can handle is 320 Arms to keep T31's junction temperature below 150°C at 22°C ambient temperature.*

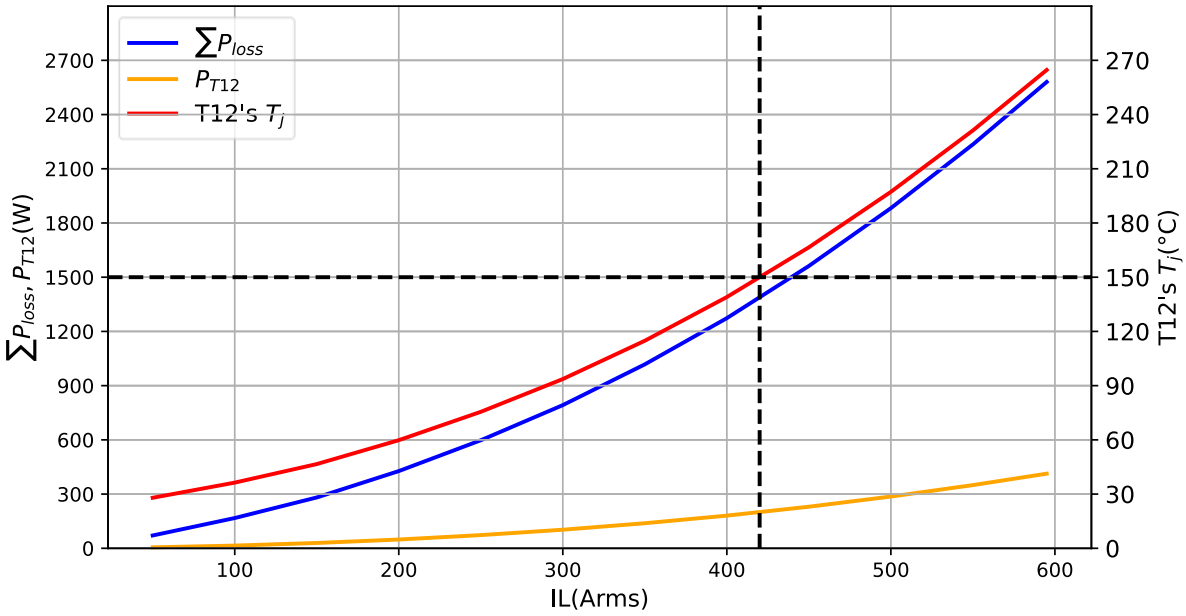


Figure 6.49: *The total losses of T12 in 4SiC hybrid ANPC at 10kHz switching frequency. The maximum load current that 4SiC ANPC can handle is 420 Arms to keep T12's junction temperature below 150°C at 22°C ambient temperature.*

Actually, 4SiC ANPC can provides more than double output current of 2SiC in some special conditions as described below:

From Figure 6.49, if a_1 is the 4SiC ANPC's average total power losses per output current (W/Arms) and a_2 is the average T12's losses per output current (W/Arms), the total losses of 4SiC ANPC and T12 can be approximated:

$$\sum P_{4SiC} = a_1 \cdot IL \tag{6.6}$$

$$P_{T12} = a_2 \cdot IL \tag{6.7}$$

In similar approach, the total losses of 2SiC ANPC and T31 can be approximated:

$$\sum P_{2SiC} = a_3 \cdot IL \tag{6.8}$$

$$P_{T31} = a_4 \cdot IL \tag{6.9}$$

The junction temperature of the SiC MOSFET in the 2SiC and 4SiC can be estimated as:

$$T_{j12} = a_1 IL \cdot Rth_{hs} + a_2 IL.Rth_{sic} + T_{ambient} \tag{6.10}$$

$$T_{j31} = a_3 IL \cdot Rth_{hs} + a_4 IL.Rth_{sic} + T_{ambient} \tag{6.11}$$

With Rth_{hs} is the heatsink steady state thermal resistance and Rth_{sic} is the steady state total thermal resistance of the SiC MOSFET including the thermal interface material. If we call the maximum load RMS current in case of 2SiC and 4SiC ANPC correspondingly are $I_{2SiCmax}$ and $I_{4SiCmax}$ when the SiC MOSFET junction temperatures reach 150°C.

$$I_{2SiCmax} = \frac{150 - T_{ambient}}{a_3 \cdot Rth_{hs} + a_4 \cdot Rth_{sic}} \tag{6.12}$$

$$I_{4SiCmax} = \frac{150 - T_{ambient}}{a_1 \cdot Rth_{hs} + a_2 \cdot Rth_{sic}} \tag{6.13}$$

The conditions for $I_{4SiCmax}$ larger than double of $I_{2SiCmax}$ is:

$$I_{4SiCmax} \geq 2I_{2SiCmax} \tag{6.14}$$

$$2(a_1 \cdot Rth_{hs} + a_2 \cdot Rth_{sic}) \leq a_3 \cdot Rth_{hs} + a_4 \cdot Rth_{sic} \tag{6.15}$$

$$(2a_1 - a_3)Rth_{hs} \leq (a_4 - 2a_2)Rth_{sic} \tag{6.16}$$

(6.16) can be written as:

$$\frac{Rth_{hs}}{Rth_{sic}} \leq \frac{a_4 - 2a_2}{2a_1 - a_3}, if\ a_1 > \frac{a_3}{2} \tag{6.17}$$

$$\frac{Rth_{hs}}{Rth_{sic}} \geq \frac{a_4 - 2a_2}{2a_1 - a_3}, if\ a_1 < \frac{a_3}{2} \tag{6.18}$$

$$k_p = \frac{a_4 - 2a_2}{2a_1 - a_3} = \frac{P_{T31} - 2P_{T12}}{2\sum P_{4SiC} - \sum P_{2SiC}} \tag{6.19}$$

k_p is the ratio of the differential losses on SiC MOSFET and the total differential losses between the 2SiC ANPC and 4SiC ANPC. Equation (6.17) shows that when the average power losses per output current of 4SiC ANPC (a_1) larger than half of that of 2SiC ANPC (a_3), the output current of 4SiC ANPC can be double current of the 2SiC ANPC when the thermal resistance ratio between the heatsink and the SiC MOSFET $\frac{Rth_{hs}}{Rth_{sic}}$ smaller than k_p. When the average power losses per output current of 4SiC ANPC (a_1) smaller than half of that of 2SiC ANPC (a_3), the output current of 4SiC ANPC can be double current of the 2SiC ANPC when the thermal resistance ratio larger than k_p, which is shown in equation (6.18).

In summary, continuous running experiments at the inverter's rated current have demonstrated that all critical components, particularly the ferrite cores and power switches, maintain temperatures within safe limits. Additionally, the parasitic turn-on optimization method and the active cut-off switching scheme have shown no issues during continuous operation. The 10kHz switching frequency is archivable at the actual air-cooling condition and semiconductors' losses.

The current setup demonstrates the superiority of 2SiC ANPC over 4SiC ANPC in terms of output current per SiC chip area. However, under certain conditions, the 4SiC ANPC configuration can outperform the 2SiC ANPC.

7. Conclusion and Future Works

7.1 Conclusion

This dissertation presents the feasibility of implementing a high-power 2SiC hybrid Si/SiC ANPC topology with a decoupling capacitor. The presence of the decoupling capacitor introduces a low resonance frequency, which can be effectively mitigated by employing an active cut-off switching scheme. The switching scheme is independent from the load current direction. However, the capacitor's voltage drifting contributes to switching losses on the IGBTs.

The long transition time of the active cut-off scheme limits the smallest available turn-on and turn-off times, leading to distortion in the load current, especially at very low or very high modulation index. To address this issue, a specialized switching schedule and fast gate discharge via C_{goff} can be utilized to reduce transition times.

Due to component tolerances and varying load conditions, the DC link voltages of the ANPC can become unbalanced. This imbalance can trigger low-frequency resonance when the converter switches between the upper and lower DC links. The amplitude of the low-frequency resonance current is directly proportional to the voltage difference between the DC links. However, the presence of a large inductance between the DC link capacitors and the decoupling capacitor helps limit the amplitude of this current. Since this effect occurs at the fundamental frequency, the switching losses on the IGBTs caused by unbalanced DC link voltages can be considered negligible. The primary concern during unbalanced switching is the potential for overvoltage when a MOSFET is triggered immediately after the zero-crossing, before the first oscillation has fully dissipated. Fortunately, in the active cut-off switching scheme, there is no oscillations being triggered during the zero-crossing, thereby avoiding this issue altogether.

Furthermore, the high frequency switching oscillations from SiC MOSFET can be efficiently suppressed by employing a skin-effect capacitor or dual soft ferrite cores. The chosen material for the cores should exhibit a sharp transition between low and high differential inductance states to prevent excessive overvoltage during SiC MOSFET turn-off. Additionally,

the core losses must be adequate within the resonance frequency range to effectively dampen switching ringing.

The snappy reverse-recovery of the SiC MOSFET's body diode can be mitigated by using the parasitic turn-on effect through adjustments in V_{gsoff} and R_{gon} parameters. The optimal combination of V_{gsoff} and R_{gon} can be determined using the methodology outlined in Chapter 5. An analytical model of reverse-recovery overvoltage and oscillations in that chapter reveals that when the SiC MOSFET is rapidly turned on, its voltage can return to zero before the reverse-recovery current returns to zero. In such cases, the overvoltage on the body diode is primarily influenced by the stray inductance of the commutation loop and the slope of the reverse-recovery current. In this case, the active clamping can be used to clamp the overvoltage of the body diode. In scenarios where the turn-on voltage reaches zero after the reverse-recovery current returns to zero, the reverse-recovery overvoltage is primarily dominated by the amplitude of oscillations. This value depends on the slope of the reverse-recovery current and the voltage slope of the turn-on device. Active clamping cannot be used in this scenario because controlling the reverse-recovery current slope is insufficient to limit the overvoltage.

The 500kW 2SiC hybrid ANPC was constructed and operated continuously at its rated current, ensuring that all critical components remained within their safe temperature limits. The thermal model indicates that the SiC MOSFETs can be switched at high speeds with minimal switching losses. However, the actual speed at which they can be switched is heavily dependent on the cooling conditions and the maximum output current of the inverter. Experimental results demonstrate that the optimization method with parasitic turn-on effects and the active cut-off switching scheme perform effectively not only during double-pulse tests but also during continuous operation.

The thermal model of the converter highlights that the 2SiC ANPC configuration surpasses the 4SiC ANPC configuration in this particular setup. However, it's worth noting that in certain conditions, the 4SiC ANPC configuration has the potential to deliver more than double the output current compared to the 2SiC ANPC.

7.2 Future works

The dissertation has achieved several significant research objectives, but there remain avenues for future development in this area:

1. Precise switching losses calculation: Developing a more accurate method for calculating the IGBT switching losses caused by decoupling capacitor voltage drift. Techniques such as utilizing lookup tables in simulation tools like PLECS could enhance the precision of these calculations.

2. Innovations in switching scheme: Continued innovation in switching schemes to mitigate decoupling capacitor voltage drift. New approaches are needed to limit this drift effectively while maintaining load current independence.

3. Ferrite core losses modeling: Developing models to accurately predict ferrite core losses, particularly in both large and small signal regions. Investigating core behavior at high temperatures is crucial for estimating core temperatures during continuous operation.

4. Power cycling investigations: Exploring the power cycling behavior of the 2SiC hybrid ANPC, considering its potential advantages in high-power density applications.

5. Back-to-back testbench development: Establishing a continuous back-to-back testbench setup to assess inverter operation under various modulation indices and operating conditions.

6. Enhanced cooling and mechanical design: Using liquid cooling systems and optimizing mechanical designs of busbars and contact terminals to increase the inverter's output current capability.

7. EMI and EMC performance analysis: Investigating the impact of high switching speeds on electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance to ensure compliance with regulatory standards.

7.3 Publications

1. P. H. Trieu To and H. -G. Eckel, "Oscillation Damping in a 500kW Hybrid Si/SiC Three-Level ANPC Inverter with Decoupling Capacitor," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. 01-10.

2. P. H. T. To, F. Kayser and H. -G. Eckel, "Turn-on Losses Optimization for Medium Power SiC MOSFET Half-bridge Module," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. P.1-P.11.

3. P. H. T. To and H. -G. Eckel, "Active Clamping for SiC MOSFET's Body Diode During Reverse-Recovery," PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2023, pp. 1-7, doi: 10.30420/566091107.

4. P. H. Trieu To and H. -G. Eckel, "Experimental 500kW Hybrid Si/SiC ANPC Inverter," PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2023, pp. 1-10, doi: 10.30420/566091086.

5. P. H. Trieu To and H. -G. Eckel, "A Simple Analytical Model for The Reverse-Recovery Overvoltage and Oscillation In a SiC MOSFET Half-Bridge Module," 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-6, doi: 10.23919/EPE23ECCEEurope58414.2023.10264503.

6. P. H. Trieu To and H. -G. Eckel, "Clean Switching of SiC MOSFET Half-Bridge Module with Soft-Ferrite Dual Cores," 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-10, doi: 10.23919/EPE23ECCEEurope58414.2023.10264462.

7. H. -G. Eckel, F. Kayser and P. H. T. To, "Hybrid Silicon-SiC Inverter – Combining the Best of Both Worlds," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. P.1-P.1.

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Appendix 1 : Coupled LCR circuit theory

The conventional 2-level inverter can be modeled with a single LC oscillator circuit. In case of 3L-TDANPC, the decoupling capacitor creates two coupled LC circuits, which has a complex analytical solution and difficult to be solved. Under certain conditions, the two coupled LC oscillators can be decoupled into two independent circuits. The solution of the whole circuit is the superposition of two individual circuits, which is easy to find. This appendix starts with the analytical solution for a single LC oscillator in different scenario. The decoupling conditions and the AC superposition theorem will be presented to produce the analytical model of the coupled LC circuit. The analytical model is verified with the simulation results.

A.1.1 Different types of LCR oscillator

A.1.1.1 Basic LC oscillator

LC oscillator in Figure A. 1.1 is frequently found in power electronics as parasitic elements of the power circuit. The waveforms of the oscillation are different depending on the initial conditions of the oscillation. Based on where the energy is stored at the beginning of the oscillation, there are 3 cases of possible initial conditions: inductance storage, capacitance storage or inductance and capacitance storage.

Case 1: Inductance storage (Figure A. 1.1a): If at t = 0, I_0 is the initial current in the inductor L, capacitor C is fully discharged $V_{cf0} = 0$. The voltage and current of the capacitor can be calculated as:

$$i_{cf}(t) = I_0 \cdot \cos(\omega t) \tag{A. 1.1}$$

$$v_{cf}(t) = I_0 \cdot \sqrt{L/C} \cdot \sin(\omega t) \tag{A. 1.2}$$

The capacitor's voltage and current can be observed from the Figure A. 1.1b, Figure A. 1.1c. With the oscillation angular frequency is

$$\omega = 1/\sqrt{LC} \tag{A. 1.3}$$

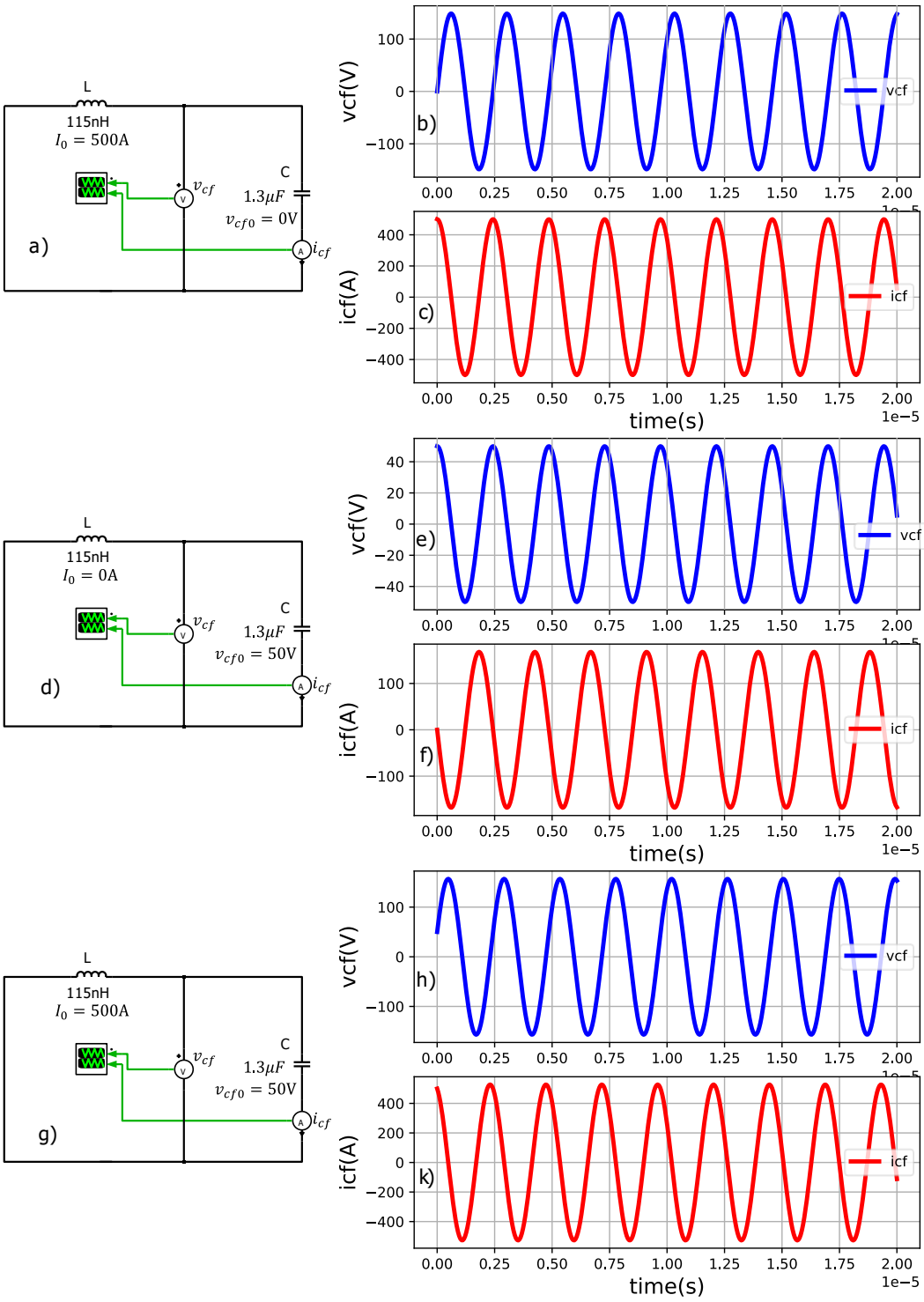


Figure A. 1.1: *LC oscillation circuit with different initial energy storage, a) inductance storage, d) capacitor storage, g) inductance and capacitance storage. Capacitor's voltage and current in case a: b, c, case d: e, f, case g:h, k.*

The initial oscillation energy which is stored in the circuit is sum of the initial capacitor's energy and initial inductor's energy.

$$E_0 = \frac{1}{2}C \cdot V_{cf0}^2 + \frac{1}{2}L \cdot I_0^2 = \frac{1}{2}L \cdot I_0^2 \quad \text{(A. 1.4)}$$

From the equation (A. 1.2), the amplitude of the voltage is smaller when bigger capacitor is used.

Case 2: Capacitance storage (Figure A. 1.1d): If at t = 0, the capacitor is charged at V_{cf0} and there is no current through the inductor, the current and voltage on the capacitor can be calculated:

$$i_{cf}(t) = \frac{-V_{cf0}}{\sqrt{L/C}} \cdot \sin(\omega t) \quad \text{(A. 1.5)}$$

$$v_{cf}(t) = V_{cf0} \cdot \cos(\omega t) \quad \text{(A. 1.6)}$$

The capacitor's voltage and current can be observed from the Figure A. 1.1e, Figure A. 1.1f

The total initial energy is equal to the initial energy of the capacitor.

$$E_0 = \frac{1}{2}C \cdot V_{cf0}^2 + \frac{1}{2}L \cdot I_0^2 = \frac{1}{2}C \cdot V_{cf0}^2 \quad \text{(A. 1.7)}$$

From equation(A. 1.5), the amplitude of the oscillation current is smaller when smaller capacitor is used.

Case 3: Inductance and capacitance storage (Figure A. 1.1g): If at t = 0, there is current I_0 goes through the inductor and the capacitor is charged to V_{cf0}, it is possible to supper position of equations (A. 1.1) and (A. 1.5), (A. 1.2) and (A. 1.6), (A. 1.4) and (A. 1.7).

$$i_{cf}(t) = I_0 \cdot \cos(\omega t) - \frac{V_{cf0}}{\sqrt{L/C}} \cdot \sin(\omega t) \quad \text{(A. 1.8)}$$

$$v_{cf}(t) = I_0 \cdot \sqrt{L/C} \cdot \sin(\omega t) + V_{cf0} \cdot \cos(\omega t) \quad \text{(A. 1.9)}$$

$$E_0 = \frac{1}{2} C \cdot V_{cf0}^2 + \frac{1}{2} L \cdot I_0^2 \qquad \text{(A. 1.10)}$$

The capacitor's voltage and current can be observed from the Figure A. 1.1h, Figure A. 1.1k.

For both 3 cases, if the stored energy in the circuit is small, the oscillation amplitudes of the voltage and current are also small. Large capacitor may reduce the oscillating voltage but it also increases the oscillating current and vice versa for the large inductance.

A.1.1.2 LC oscillator with DC voltage source

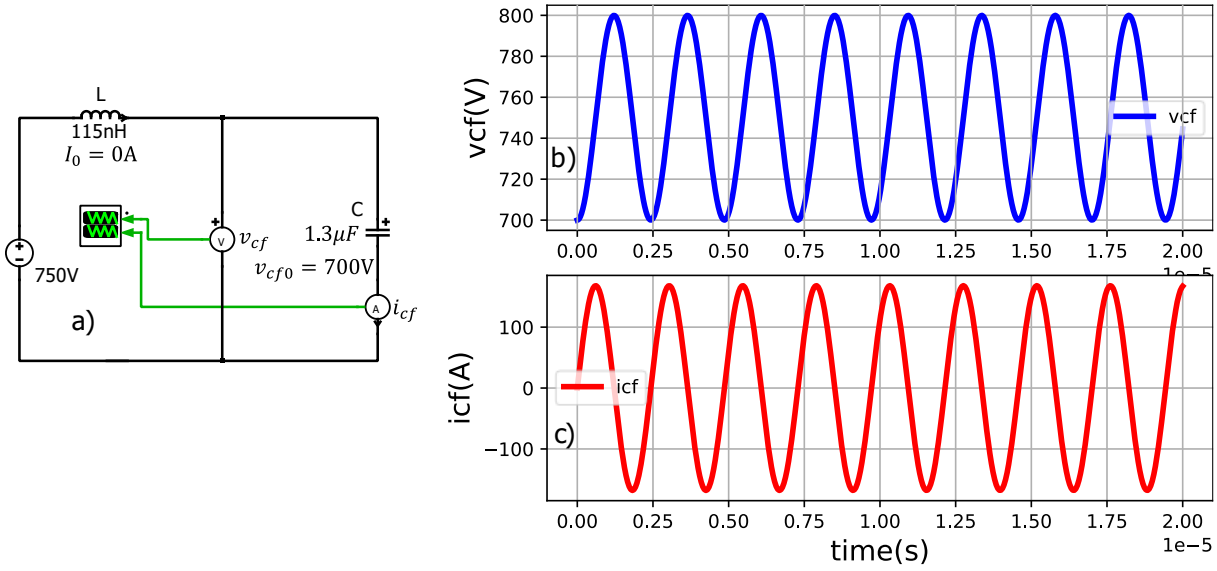


Figure A. 1.2: *a) LC oscillator with DC voltage in the circuit. b, c) voltage and current of the capacitor*

In practical circuit, there is usually a DC voltage source connected in the oscillation circuit like Figure A. 1.2a. The DC voltage source creates a new equilibrium voltage level at the capacitor. If at t = 0, there is current I_0 goes through the inductor and the capacitor is charged to V_{c0}, the voltage and current on the capacitor are:

$$i_{cf}(t) = I_0 \cdot \cos(\omega t) - \frac{V_{cf0} - V_{DC}}{\sqrt{L/C}} \cdot \sin(\omega t) \qquad \text{(A. 1.11)}$$

$$v_{cf}(t) = I_0 \cdot \sqrt{\frac{L}{C}} \cdot \sin(\omega t) + (V_{cf0} - V_{DC}) \cdot \cos(\omega t) + V_{DC} \quad \text{(A. 1.12)}$$

$$E_0 = \frac{1}{2} C \cdot (V_{cf0} - V_{DC})^2 + \frac{1}{2} L \cdot I_0^2 \quad \text{(A. 1.13)}$$

If the initial voltage of the capacitor $V_{cf0} = 700V$, V_{DC} = 750V. The capacitor's voltage and current can be seen in the Figure A. 1.2b, Figure A. 1.2c. The initial oscillation energy is proportional to $(V_{cf0} - V_{DC})^2$.

A.1.1.3 LCR oscillator

The LC oscillators that are described above are ideal oscillators. In real applications, there is always a resistance in the circuit even though it may be a small value (Figure A. 1.3a).

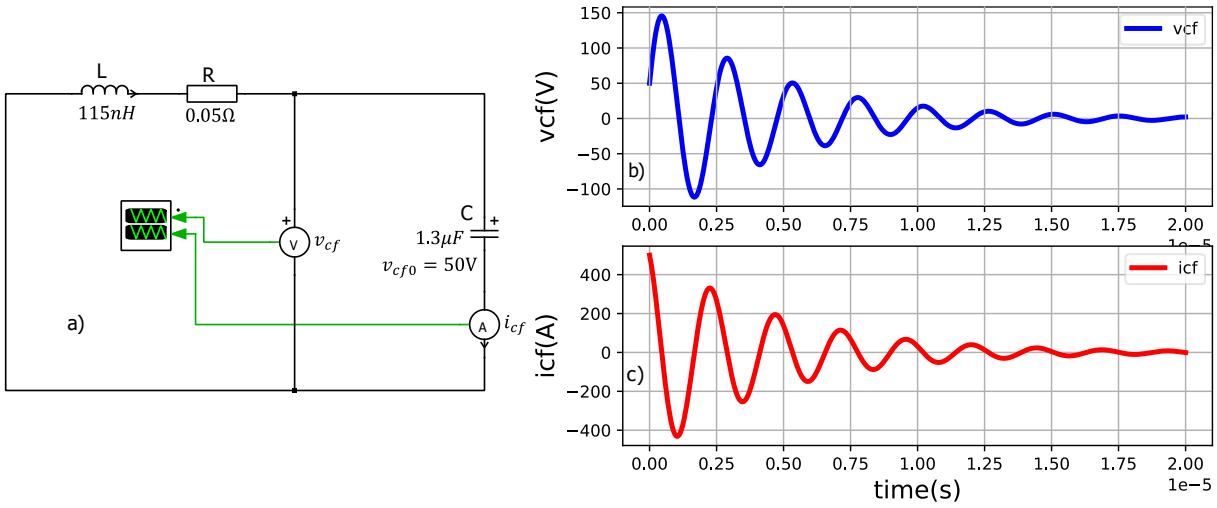


Figure A. 1.3: a) *LCR oscillation circuit. b, c) Capacitor's voltage and current.*

The difference from LCR oscillator and LC oscillator is that the energy that stored in the oscillation circuit will be dissipated on the resistor of the circuit at the rate $e^{-tR/L}$:

$$E(t) = E_0 \cdot e^{-tR/L} \quad \text{(A. 1.14)}$$

And hence the amplitude of the voltage and current are reduced at rate $e^{-tR/2L}$:

$$i_{cf}(t) = \left(I_0 \cdot \cos(\omega' t) - \frac{V_{cf0}}{\sqrt{L/C}} \cdot \sin(\omega' t) \right) \cdot e^{-tR/2L} \quad \text{(A. 1.15)}$$

$$v_{cf}(t) = \left(I_0 \cdot \sqrt{\frac{L}{C}} \cdot \sin(\omega' t) + V_{cf0} \cdot \cos(\omega' t) \right) \cdot e^{-tR/2L} \quad \text{(A. 1.16)}$$

The ratio $\alpha = R/2L$ is called the attenuation factor. If the oscillator has a larger resistor, the oscillation energy is dissipated faster and hence the oscillation is attenuated faster. The angular frequency in LCR circuit is slightly different from LC circuit. In most cases, R is small enough so that:

$$\omega' = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \approx \sqrt{\frac{1}{LC}} \quad \text{(A. 1.17)}$$

To characterize the oscillating conditions, the damping factor ζ is defined as:

$$\zeta = \frac{\alpha}{\omega'} = \frac{R}{2} \cdot \sqrt{\frac{C}{L}} \quad \text{(A. 1.18)}$$

If $\zeta = 0$: undamped oscillation. In this condition, the oscillation's energy is not dissipated.

If $1 > \zeta > 0$: under damped oscillation. The oscillation's energy in this condition is dissipated by the resistance. The larger ζ is the faster the oscillation is damped.

If $\zeta = 1$: critical damped oscillation: this is the border between the oscillation and non-oscillation circuit.

If $\zeta > 1$: overdamped oscillation: there is no oscillation starts in the circuit.

A.1.2 Decoupling of two coupled LCR networks

When there are two or more LCR circuits which are connected in cascaded like in Figure A. 1.4, the analytical solutions are very complicated because of the high order differential equations. To simplify the analytical solution, it is necessary to decouple the circuit into two

independent LCR circuits so the analytical solution for each LCR circuit can be solved independently.

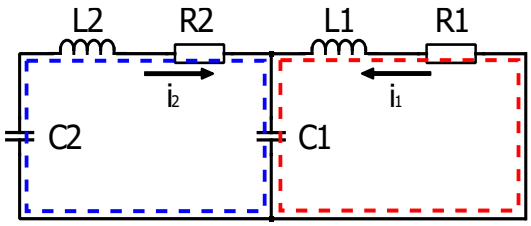


Figure A. 1.4:*Two coupled LCR circui t: $L_1C_1R_1$ and $L_2C_2R_2$.*

Two coupled LCR networks are decoupled when they oscillate at their own resonance frequency and their resonance current run locally in their own circuit. The conditions for decoupling two coupled $L_1C_1R_1$ and $L_2C_2R_2$ in Figure A. 1.4 are:

At the resonance frequency $\omega_1 = 1/\sqrt{L_1C_1}$, to have the oscillation current i_1 runs locally in $L_1C_1R_1$ circuit, the impedance of the capacitor C1 has to be satisfied:

$$|Z_{c1}(\omega_1)| \ll \left|R_2 + jL_2\omega_1 - \frac{j}{C_2\omega_1}\right| \tag{A. 1.19}$$

To simplify the calculation, it is assumed that R_2 is small and neglectable. If $k_{dc} > 1$ is a decoupling factor, which defines how much the circuit $L_1C_1R_1$ is decoupled from $L_2C_2R_2$ or how much the current i_1 flows through the capacitor C1 compare to the current through $L_2C_2R_2$, equation (A. 1.19) can be rewritten as:

$$\left|\frac{j}{C_1\omega_1}\right| \cdot k_{dc} = \left|jL_2\omega_1 - \frac{j}{C_2\omega_1}\right| \tag{A. 1.20}$$

$$C_1 = \frac{k_{dc} \cdot C_2}{\left|\frac{L_2C_2}{L_1C_1} - 1\right|} \tag{A. 1.21}$$

If it is assumed that $\omega_2 \gg \omega_1$,

$$L_2C_2 \ll L_1C_1 \tag{A. 1.22}$$

$$\left|\frac{L_2C_2}{L_1C_1} - 1\right| \approx 1 \tag{A. 1.23}$$

Replace (A. 1.23) to (A. 1.21) $C_1 = k_{dc} \cdot C_2$ (A. 1.24)

Replace (A. 1.24) to (A. 1.22)

$$k_{dc} \gg \frac{L_2}{L_1} \quad \text{(A. 1.25)}$$

At the resonance frequency $\omega_2 = 1/\sqrt{L_2 C_2}$, to have the oscillation current i_2 runs locally in $L_2C_2R_2$ circuit, the impedance of the capacitor C1 has to satisfy:

$$|Z_{c1}(\omega_2)| \ll |R_1 + jL_1\omega_2| \quad \text{(A. 1.26)}$$

If R_1 is small and neglectable and k_{dc} is decoupling factor,

$$\left|\frac{-j}{C_1\omega_2}\right| \cdot k_{dc} = |jL_1\omega_2| \quad \text{(A. 1.27)}$$

$$C_1 = k_{dc} \cdot \frac{L_2}{L_1} \cdot C_2 \quad \text{(A. 1.28)}$$

If $L_2 < L_1$, from (A. 1.24), (A. 1.25) and (A. 1.28), the condition for decoupling two coupled $L_1C_1R_1$ and $L_2C_2R_2$ are:

$$C_1 = k_{dc} \cdot C_2 \text{ with } k_{dc} \gg \frac{L_2}{L_1} \; and \; L_2 < L_1 \quad \text{(A. 1.29)}$$

A.1.3 Superposition of AC circuit theorem

In the coupled LCR circuit, if $L_1C_1R_1$ and $L_2C_2R_2$ are fully decoupled: $C_1 = k_{dc} \cdot C_2$ with $k_{dc} \gg \frac{L_2}{L_1}, L_2 < L_1$, the superposition of AC circuit theorem can be applied. In the superposition theorem for AC circuit, if the circuit operates at different frequencies, the respond of the circuit is the superposition of its responds in the equivalent circuits at different frequencies [37]. In frequency domain, at the low frequency ω_1, the impedance of the capacitor C2 is very large in compare to C1's impedance so it can be replaced with open circuit (Figure A. 1.5b). At the high frequency ω_2, the capacitor C1's impedance is very small compare to C2'impedance and it can be considered as a short-circuit (Figure A. 1.5c). The oscillation voltage on capacitor C2 is the superposition of its voltage at frequency ω_1: $v_{c2}(\omega_1 t)$ and its voltage at frequency ω_2:

$v_{c2}(\omega_2 t)$. The voltage $v_{c2}(\omega_1 t) = v_{c1}(\omega_1 t)$ because C2 is opened circuit at frequency ω_1. The voltage and current through the capacitor C2 are:

$$v_{c2}(t) = v_{c2}(\omega_1 t) + v_{c2}(\omega_2 t) \quad \text{(A. 1.30)}$$

$$i_{c2}(t) = i_{c2}(\omega_2 t) \quad \text{(A. 1.31)}$$

Because C2 is opened at frequency ω_1 (Figure A. 1.5b)

$$v_{c2}(\omega_1 t) = v_{c1}(\omega_1 t), \text{ and } i_{c2}(\omega_1 t) = 0 \quad \text{(A. 1.32)}$$

$$v_{c2}(t) = v_{c2}(\omega_1 t) + v_{c2}(\omega_2 t) = v_{c1}(\omega_1 t) + v_{c2}(\omega_2 t) \quad \text{(A. 1.33)}$$

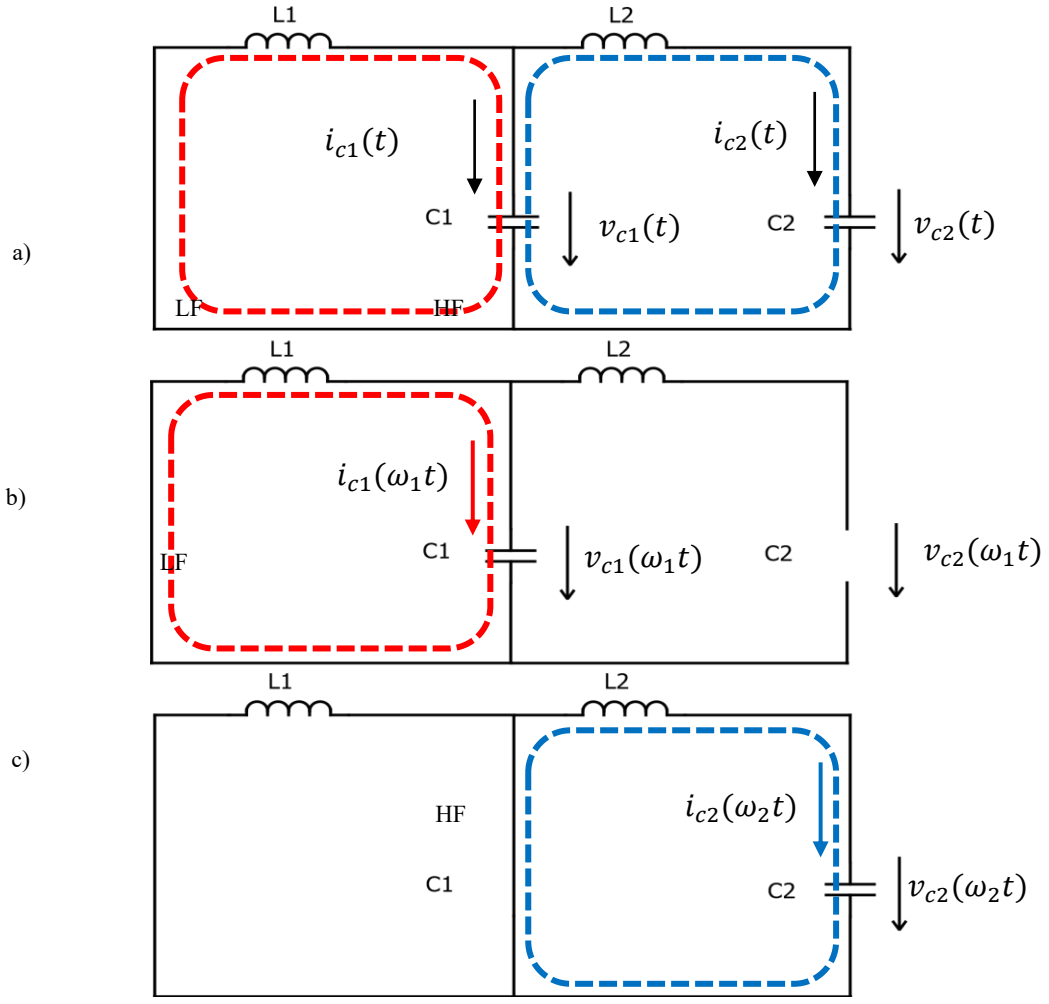


Figure A. 1.5: *The coupled LCR oscillator. a) equivalent circuit in time domain, b) equivalent oscillation circuit at low frequency ω_1, c) equivalent oscillation circuit at high frequency ω_2.*

The voltage and current through the capacitor C1 are:

$$i_{c1}(t) = i_{c1}(\omega_1 t) - i_{c2}(\omega_2 t) \tag{A. 1.34}$$

$$v_{c1}(t) = v_{c1}(\omega_1 t) \tag{A. 1.35}$$

If we assume that at t = 0, the capacitor C_1, C_2 are charged at V_{c10}, V_{c20} and the current through L_1, L_2 is I_L. The initial phase of the two corresponding oscillations are φ_1, φ_2.

$$v_{c1}(t) = I_L \cdot \sqrt{\frac{L_1}{C_1}} \cdot \sin(\omega_1 t + \varphi_1) + V_{c10} \cdot \cos(\omega_1 t + \varphi_1) \tag{A. 1.36}$$

$$v_{c2}(t) = v_{c1}(t) + \left(I_L \sqrt{\frac{L_2}{C_2}} \sin(\omega_2 t + \varphi_2) + V_{c20} \cos(\omega_2 t + \varphi_2) \right) \tag{A. 1.37}$$

$$i_{c2}(t) = I_L \cdot \cos(\omega_2 t + \varphi_2) - \frac{V_{c20}}{\sqrt{\frac{L_2}{C_2}}} \cdot \sin(\omega_2 t + \varphi_2) \tag{A. 1.38}$$

$$i_{c1}(t) = I_L \cdot \cos(\omega_1 t + \varphi_1) - \frac{V_{c10}}{\sqrt{\frac{L_1}{C_1}}} \cdot \sin(\omega_1 t + \varphi_1) - i_{c2}(t) \tag{A. 1.39}$$

A.1.4 Verification of the coupled LCR oscillator model with SIMetrix simulation.

To verify the analytical model of the coupled LCR oscillator which is proposed in previous section, a SIMetrix simulation is created like in Figure A. 1.6 with the parameters: $L_1 = 119nH, R_1 = 50m\Omega, C_1 = 1.5\mu F, L_2 = 46nH, R_2 = 300m\Omega, C_2 = 1.85nF, V_{DC} = 750V, I_L$= 600A. The decoupling condition $C_1 = 810 \cdot C_2$ with $k_{dc} = 810 \gg \frac{L_2}{L_1} = 0.38$. To mimic the switching conditions in ANPC, the initial voltage on C1 is set at 750V, the initial voltage on C2 is 0V, the initial current of L_1, L_2 is I_L = 600 A. Voltage and current of the capacitor C1, C2 are VC1, VC2, IC1, IC2 are measured and displayed in Figure A. 1.7. The analytical model for this simulation circuit in Figure A. 1.6 are:

$$v_{c1}(t) = I_L \cdot \sqrt{\frac{L_1}{C_1}} \cdot \sin(\omega_1 t) \cdot e^{\frac{-R_1}{2L_1}t} + (V_{c10} - V_{DC}) \cdot \cos(\omega_1 t) \cdot e^{\frac{-R_1}{2L_1}t} + V_{DC} \quad \text{(A. 1.40)}$$

$$v_{c2}(t) = v_{c1}(t) + I_L \cdot \sqrt{\frac{L_2}{C_2}} \cdot \sin(\omega_2 t) \cdot e^{\frac{-R_2}{2L_2}t} + V_{c20} \cdot \cos(\omega_2 t) \cdot e^{\frac{-R_2}{2L_2}t} \quad \text{(A. 1.41)}$$

$$i_{c2}(t) = I_L \cdot \cos(\omega_2 t) \cdot e^{\frac{-R_2}{2L_2}t} - \frac{V_{c20}}{\sqrt{\frac{L_2}{C_2}}} \cdot \sin(\omega_2 t) \cdot e^{\frac{-R_2}{2L_2}t} \quad \text{(A. 1.42)}$$

$$i_{c1}(t) = I_L \cdot \cos(\omega_1 t) \cdot e^{\frac{-R_1}{2L_1}t} - \frac{(V_{c10} - V_{DC})}{\sqrt{\frac{L_1}{C_1}}} \cdot \sin(\omega_1 t) \cdot e^{\frac{-R_1}{2L_1}t} - i_{c2}(t) \quad \text{(A. 1.43)}$$

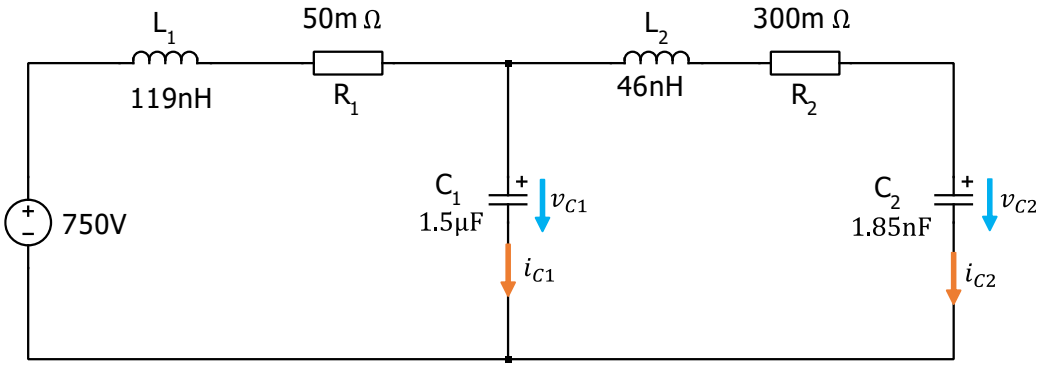


Figure A. 1.6: *SIMetrix simulation of the coupled LCR oscillator.*

Figure A. 1.8 plots the waveform of voltage and current on the capacitor C1 and C2 from the equation (A. 1.40), (A. 1.41), (A. 1.42), (A. 1.43). It can be seen that the proposed analytical model predicts quite well the voltage and current of the simulation model.

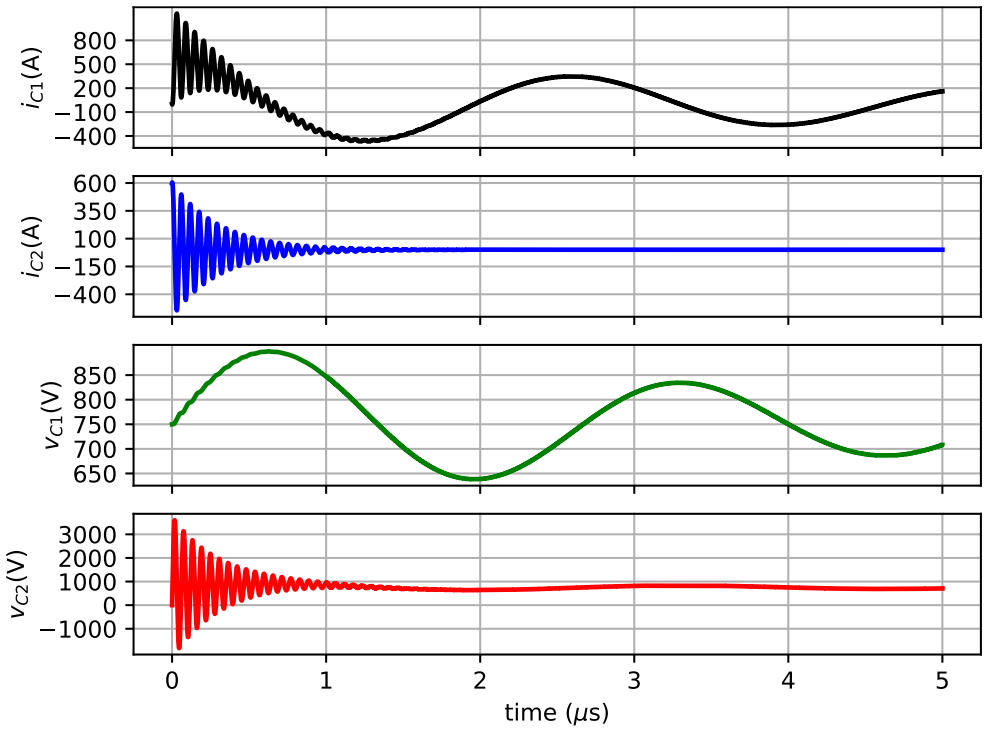


Figure A. 1.7: *SIMetrix simulation result of the coupled LCR oscillator.*

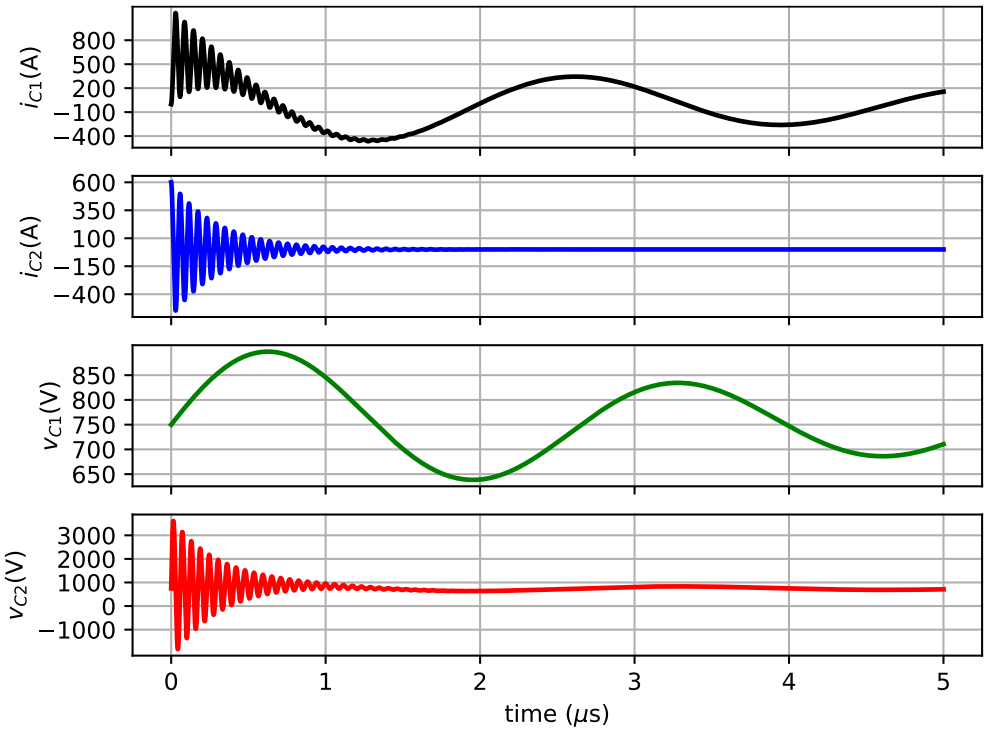


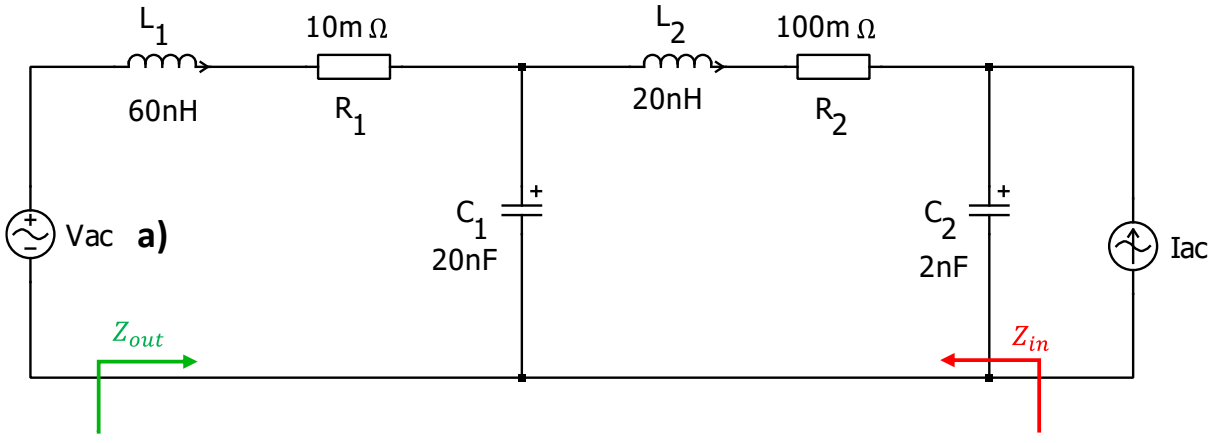
Figure A. 1.8: *Analytical result of the proposed model for the simulation circuit in Figure A. 1.6.*

A.1.5 Oscillation trigger mechanisms

An oscillation circuit can actually be considered as a two-ports impedance network which may has different input and output frequency responds [101]. For example, a coupled LCR network in Figure A. 1.9a will have the frequency responds like Figure A. 1.9b. The input impedance spectrum of the circuit shows 2 peaks at two resonance frequencies f_{rs1}, f_{rs2}. If there are current excitation sources at the input, which have the same resonance frequencies f_{rs1}, f_{rs2}, the resonance input voltages of the circuit will be amplified. In contrast, the output impedance spectrum of the circuit shows only one valley at resonance frequency f_{rs1}. If there is a voltage excitation source at the output of the circuit, which has the same resonance frequency f_{rs1}, the output resonance current will be amplified. In the real applications, those excitation sources are actually the voltage slopes and current slopes, which have the frequency spectrums include also the resonance frequencies of the circuit.

For easy understanding, let's define the input of the circuit is parallel with the capacitor and the output of the circuit is in series with the inductor and resistor. With this definition, the input impedance has two peaks at both low and high resonance frequency. While the output impedance has only one valley at the low resonance frequency. The difference between the input and output impedance spectrum has some interesting consequences:

- Only current slope at the input of the circuit can trigger the oscillation and both the low frequency and high frequency loops are triggered.
- Only voltage slope at the output of the circuit can trigger the oscillation and only the low frequency is triggered.



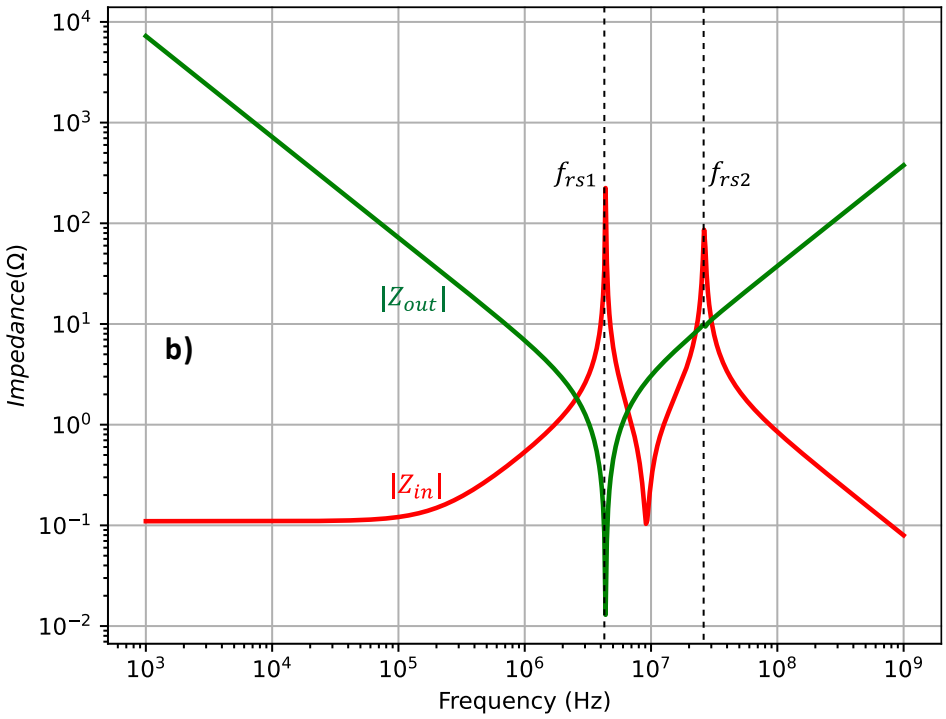


Figure A. 1.9: *a) a coupled LCR network and b) its input impedance (red line) and output impedance (green line) in the frequency domain.*

A.1.5.1 Voltage slope at the output

In the inverter applications, the voltage slope excitation at the output has many different variants. Some common variants are shown in Figure A. 1.10. The first simple form is Figure A. 1.10a, in which, the capacitor has its initial voltage V_{cf0}. The voltage slope is generated when the switch S2 are closed and the voltage on the capacitor falls to zero. In the second form (Figure A. 1.10b), there is a DC voltage source which has the voltage $V_{DC}/2$, the capacitor is charged to V_{cf0}. When the switch S2 is closed, the voltage slope is generated only when $V_{cf0} \neq V_{DC}/2$. If $V_{cf0} > V_{DC}/2$, the falling slope is generated and if $V_{cf0} < V_{DC}/2$, the rising slope is generated. This form is usually observed in the hybrid ANPC, when one of the IGBT is closed and the decoupling capacitor is charged to a certain voltage different from the $V_{DC}/2$. The falling edge will discharge the capacitor and vice versa. Another variant of the voltage slope is depicted in Figure A. 1.10c, the circuit consists of two different DC voltage sources at the output of the circuit. The switches S1, S2 are switched at the same time to connect the oscillation circuit with the DC voltage sources. For example, at the beginning, S1, S2 connect the circuit to V_{DC1}, at the steady state when all the oscillation is died out, the voltage on the capacitor is

charged to V_{DC1}. When the switches S1, S2 are switched to connect the oscillation circuit to the V_{DC2}, the voltage slope is generated if $V_{DC1} \neq V_{DC2}$. If $V_{DC1} > V_{DC2}$, the falling slope is generated and vice versa. The oscillation energy is proportional to the $\left(V_{DC_1} - V_{DC_2}\right)^2$. This type of voltage slope is usually observed when there is an unbalanced DClink voltage of the ANPC which is mentioned in chapter 2.

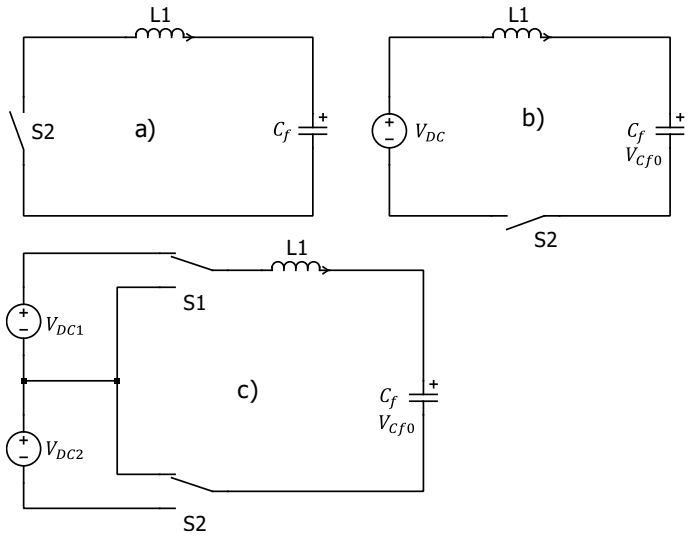


Figure A. 1.10: *Different variants of the voltage slope trigger the oscillation at the output of the oscillator.*

A.1.5.2 Current slope at the input

A current slope excitation at the input of a coupled LC circuit is usually observed during the current transient of the MOSFET with decoupling capacitor C_f like in Figure A. 1.11a. The small signal model of the MOSFET can be considered as a current slope in parallel with its output capacitor [101]. During the MOSFET's turn-off, the current slope is the channel current and during the reverse-recovery, the current slope is the reverse-recovery current of the body diode.

The current slope triggers both low and high resonance frequencies which are two impedance peaks in the spectrum. A simulation result of the circuit in Figure A. 1.11a shows the current and voltage waveforms of the decoupling capacitor C_f and the MOSFET's output capacitor C_{oss} in Figure A. 1.11b,c. The result satisfies the decoupling theory presented above:

- Because C_f has low impedance at high frequency, v_{cf} contains only the low frequency component and i_{cf} contains both the low and high frequency components.
- Because C_{oss} has high impedance at low frequency, v_{coss} contains both the low and high frequency components and i_{coss} contains only the high frequency component.

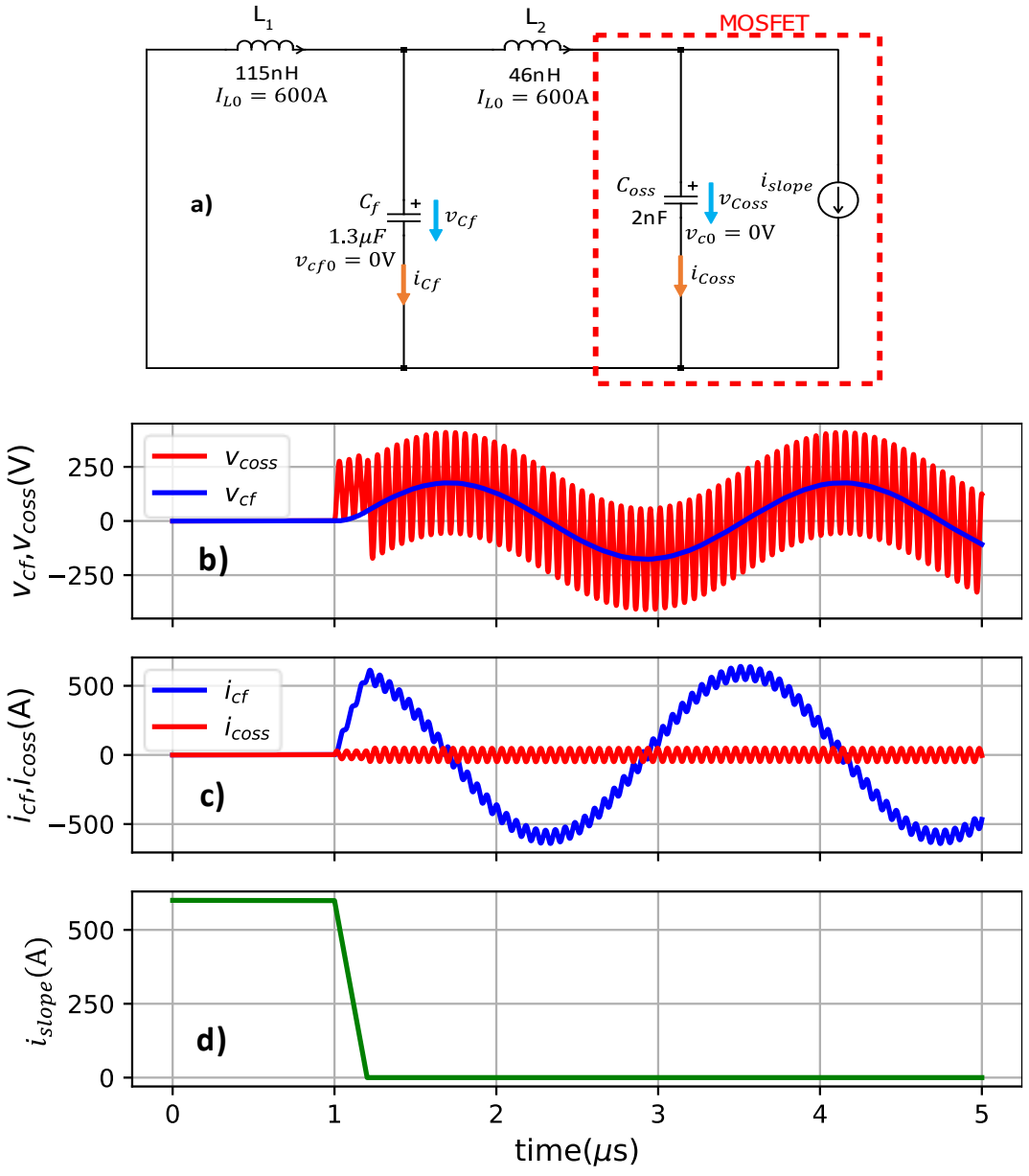


Figure A. 1.11: *Small signal simulation of current slope trigger at the input of the coupled LC circuit.*

A.1.6 Stray inductance decoupling condition

When there is a current slope at the output of a LC circuit, its commutation path depends on its bandwidth and the impedance distribution of the circuit. A rising current slope's bandwidth (BW) can be approximated from its rising time t_r [113, 114]:

$$BW = \frac{0.35}{t_r} \tag{A. 1.44}$$

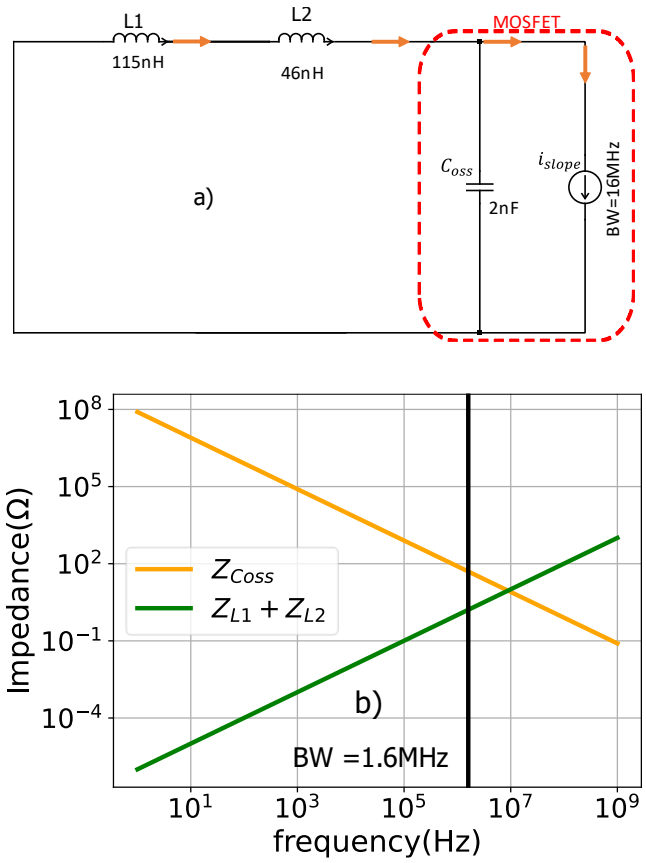


Figure A. 1.12: *a) Current slope at the input of an LC circuit without decoupling capacitor. b) The impedance spectrum of L_1+L_2 and C_{oss} at the frequency bandwidth of the current slope i_{cn}, BW = 1.6MHz, L_1+L_2 = 161nH, C_{oss} = 2nF, Z_{L1}+Z_{L2} ≪ Z_{Coss}.*

In case of FF3MR12KM1P, the typical rising time is 219ns [109], its bandwidth is around 1.6MHz. If there is no decoupling capacitor in the circuit, the impedance $Z_{L1} + Z_{L2} \ll Z_{Coss}$ at the bandwidth (BW) frequency as can be seen in Figure A. 1.12a. The transient current goes fully through both L_1, L_2, there is almost no current flows through C_{oss}. The commutation loop's inductance is large, which leads to high overvoltage.

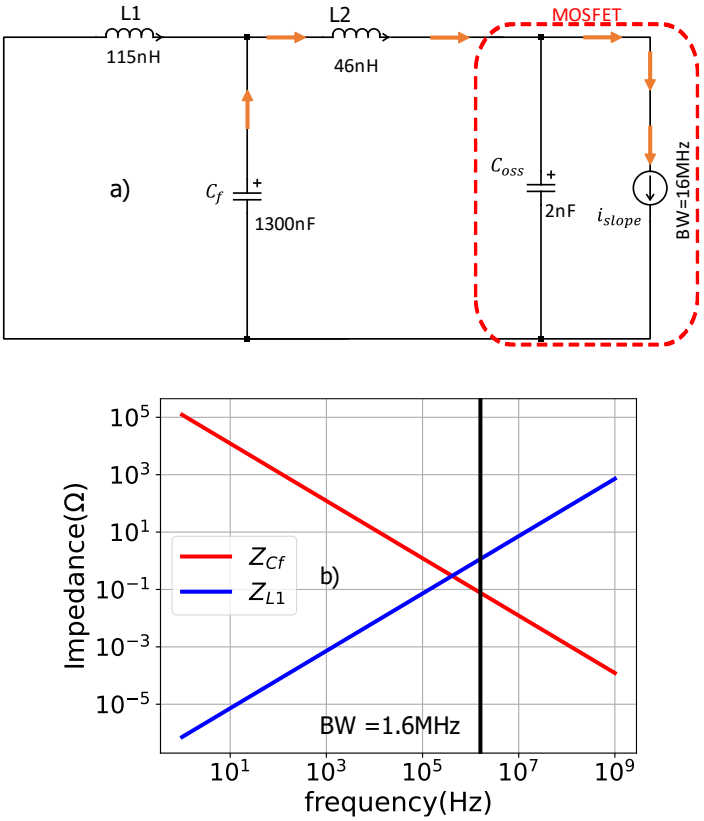


Figure A. 1.13: *a) Current slope at the input of a coupled LC circuit formed by inserting a decoupling capacitor C_f. The impedance of L_1 and C_f at the frequency bandwidth of the current slope i_{cn}, BW = 1.6MHz, L_1 = 115nH, C_f = 1.3µF, $Z_{Cf} \ll Z_{L1}$.*

If there is a decoupling capacitor C_f which is large enough like in the Figure A. 1.13a, the impedance $Z_{Cf} \ll Z_{L1}$ at the bandwidth frequency (BW) as shown in Figure A. 1.13b. The transient current now goes fully through L_2, C_f instead of L_1, L_2. Consequently, the large inductance $L_1 + L_2$ is decoupled into L_2. The commutation loop's inductance now is smaller with lower overvoltage. Depending on the current slope's bandwidth BW, decoupling capacitor's value needed to decouple the inductance L_1 is:

$$\frac{1}{2\pi \cdot BW \cdot C_f} \ll 2\pi \cdot BW \cdot L_1 \tag{A. 1.45}$$

$$C_f \gg \frac{0.2 \cdot t_r^2}{L_1} \tag{A. 1.46}$$

Appendix 2 : 2SiC Hybrid ANPC Hardware and Software Design

A.2.1 DC link capacitor selection

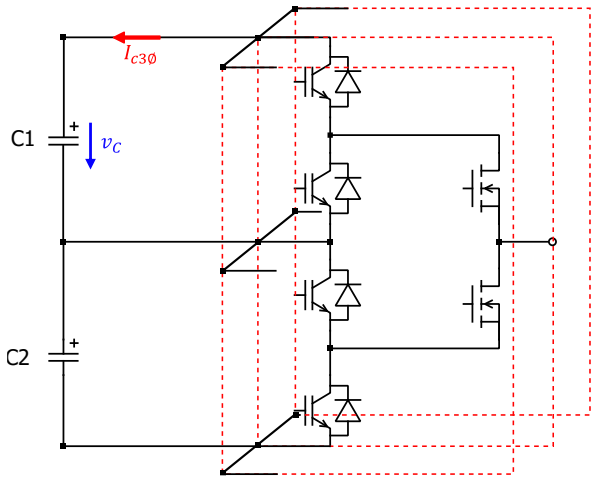


Figure A. 2.1: *3 phases ANPC and 3-phases DC link capacitor current.*

DC link capacitor is one of the important parts of the inverter, which buffers the energy from the input to the output of the inverter. The selection of DC link capacitors mainly focuses on calculating its RMS current which depends on the type of the modulation, topology, power factor and the output current [85, 86, 88, 94]. For the 3-level, 3-phase inverter which uses sine-triangle PWM, Gopalakrishnan proposed the analytical calculation of the DC link capacitor RMS current in [88].

$$I_{c3\emptyset} = \sqrt{\frac{3I_m^2 M}{4\pi}\left(\sqrt{3} + \frac{2}{\sqrt{3}}(2\cos^2(\phi) - 1)\right) - \frac{9}{16}(I_m M)^2 \cos^2(\phi)} \quad \text{(A. 2.1)}$$

With I_m is the output phase current amplitude, M is the modulation index, $\cos(\phi)$ is the power factor. At I_m = 450A, $\cos(\phi) = 0.96$, the maximum RMS current goes through the capacitor is 203Arms at M = 0.63.

The capacitor's voltage ripple ΔV_c can be estimated from the equation:

$$i_{C1}(t) = C_1 \frac{dv_c}{dt} \quad \text{(A. 2.2)}$$

$$\Delta V_c \approx \frac{I_{C3\emptyset} \cdot \Delta t}{C_1} \tag{A. 2.3}$$

The capacitor value needed to limit the voltage ripple ΔV_c at the switching frequency $f_{sw} = \frac{1}{\Delta t}$

$$C_1 \geq \frac{I_{C3\emptyset}}{\Delta V_c \cdot f_{sw}} \tag{A. 2.4}$$

Table A. 2.1: *DC link capacitor specifications [84].*

U_N(V)	C(µF)	ESR(mΩ)	ESL(nH)	Max Irms (A)	Ipeak(kA)	Max surge Current (kA)
900	409	0.94	25	70	3.6	10.7

At high switching frequency, capacitor value needed to stable the DC link is small. At the switching frequency $f_{sw} = 10kHz$, the DC link capacitor (C1) can be flexibly chosen at 2.4 mF which is enough to have a stable DC link voltage with the maximum ripple around 8V. In one phase of this hybrid ANPC, two of 900V-409μF metal film capacitors in parallel are used as $\frac{1}{3}C1$. The specifications of the capacitor can be seen in Table A. 2.1.

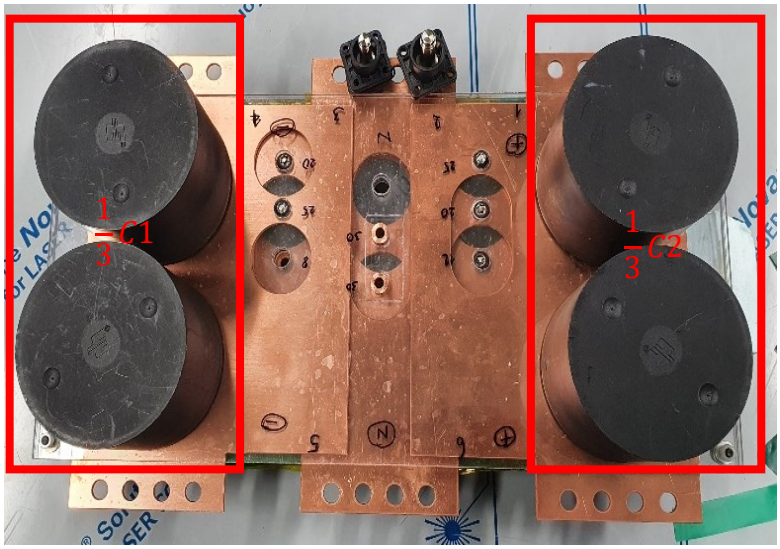


Figure A. 2.2: *DC link capacitors for 1 phase of the hybrid ANPC.*

A.2.2 Power switches selection

One phase of the hybrid ANPC including: two 62 mm module IGBTs: FF600R12KT4, 1200V- 600A, and one 62mm module SiC MOSFET: FF3MR12KM1P, 1200V-375A.

Table A. 2.2: *The nominal switching parameters of SiC MOSFET: FF3MR12KM1P [109].*

I_{nom} (A)	V_{DC} (V)	Lσ (nH)	Tj (°C)	V_{gs} (V)	R_{gon} (Ω)	R_{goff} (Ω)	di/dt(on) (A/ns)	du/dt(off) (V/ns)	Eon (mJ)	Eoff (mJ)
375	600	20	150	-5/15	4.3	3.6	7.05	7.76	16	13.5

Table A. 2.3: *The nominal switching parameters of the IGBT: FF600R12KT4 [69].*

I_{nom} (A)	V_{DC} (V)	Lσ (nH)	Tj (°C)	V_{gs} (V)	R_{gon} (Ω)	R_{goff} (Ω)	di/dt(on) (A/ns)	du/dt(off) (V/ns)	Eon (mJ)	Eoff (mJ)
600	600	20	150	-15/15	0.62	0.62	11	3.6	35.5	82

Table A. 2.4: *The nominal switching parameters of the diode in FF600R12KT4 [69].*

I_F (A)	VR (V)	Lσ (nH)	Tj (°C)	VF (V)	IFRM (A)	di_F/dt (A/ns)	Qr (μC)	Err (mJ)	I_{RM} (A)
600	600	20	150	1.75	1200	-11	110	54.5	680

A.2.3 Inverter layout

The inverter has 6 main links: DC+, DC-, neutral, upper, lower and AC like in the Figure A. 2.3. It is important to have the symmetrical layout for the upper and lower links and as well as the upper DC link and lower DC link of the inverter. The IGBT half-bridge HB1 and DC link capacitor C1, C2 are on the upper loop of the ANPC. The IGBT half-bridge HB2 and DC link capacitor C3, C4 are on the lower loop of the ANPC. The SiC MOSFET HB3 is in the

middle between HB1, HB2. To have symmetrical loops of the upper and lower ANPC, HB3 is rotated in the opposite direction of HB1 and HB2.

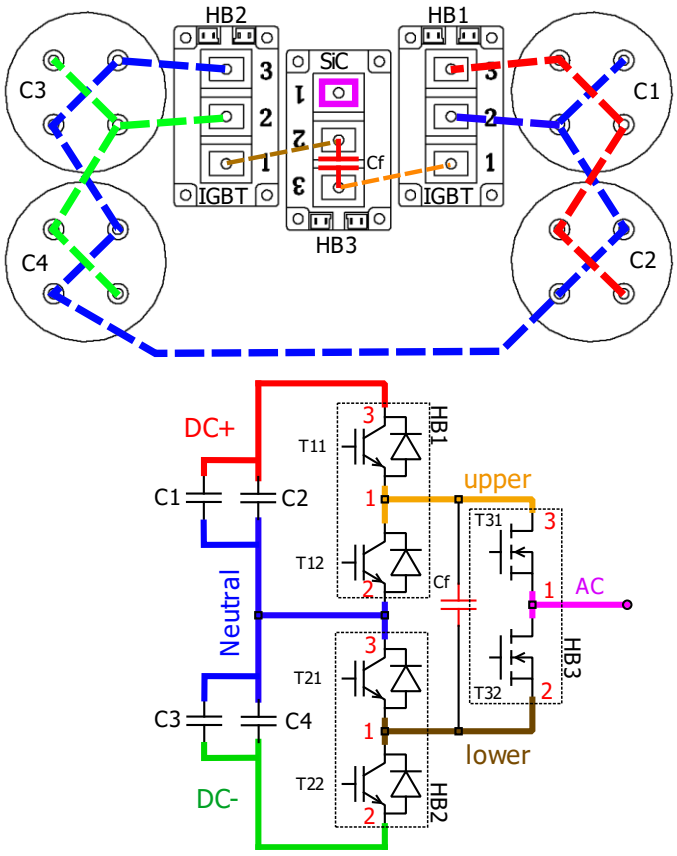


Figure A. 2.3: *Single phase layout of the hybrid ANPC inverter.*

The busbar will be the dashed lines that connects all the components. It can be seen that the busbar structure is complex and it includes also the AC terminals of HB1, HB2 which is not optimized for low inductance during the module manufacturing. The unavoidable consequence of this complex structure is the high inductance commutation loops. The decoupling capacitor is installed on top of the busbar between the terminal 2, 3 of HB3 to decouple the large commutation loop of SiC MOSFET.

A.2.4 Busbar design

The busbar consists of 5 main copper plates which are isolated by 3 isolation layers (Figure A. 2.3). The measurement of different commutation loops' inductance in the hybrid ANPC can be seen in the Figure A. 2.5. The busbar stack is presented in Figure A. 2.4. The parasitic inductances of the commutation loop's components are outline in Table A. 2.5.

Table A. 2.5: *The internal inductance of the hybrid ANPC components.*

	Inductance (nH)
DC link capacitor	25
62mm Module	20
Film decoupling capacitor	21
Conduction cooled decoupling capacitor	3
One 8mm distance bolt	6.4

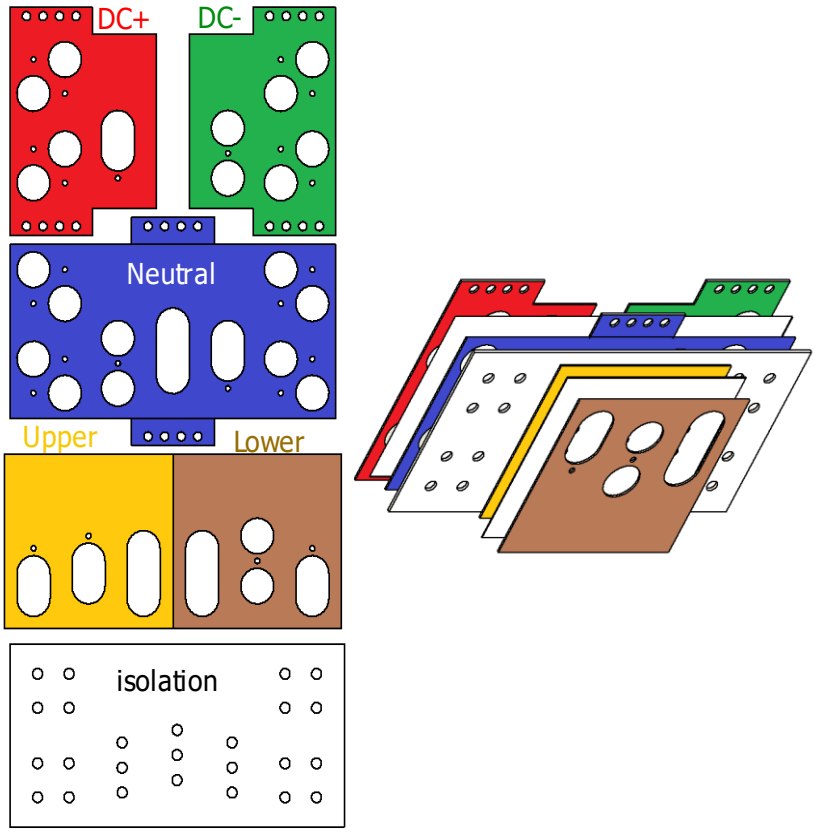


Figure A. 2.4: *Busbar layers and their arrangement.*

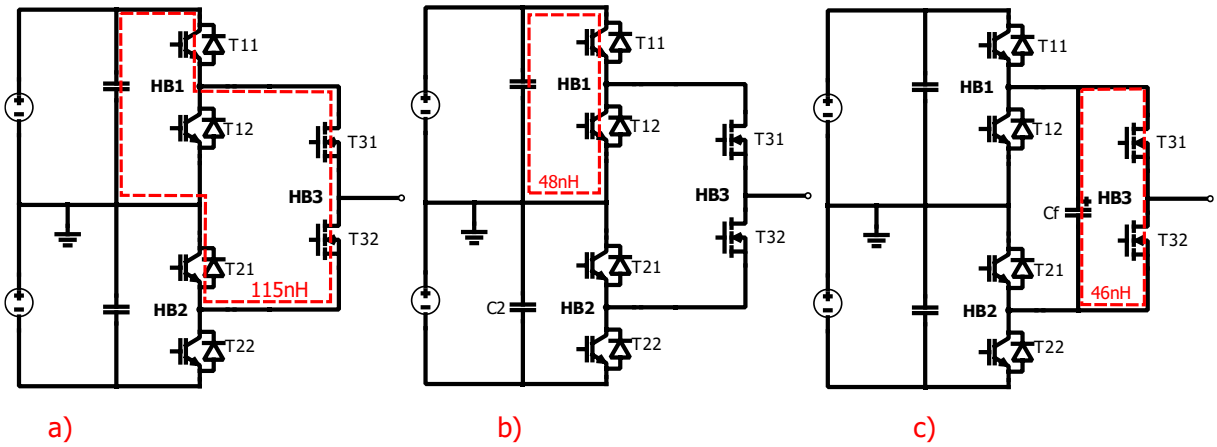


Figure A. 2.5:*Different commutation loops' inductance in the hybrid ANPC. a) MOSFET commutation loop without decoupling capacitor: 115nH, b) IGBT's commutation loop: 48nH, c) MOSFET commutation loop with decoupling capacitor: 46nH.*

A.2.5 Decoupling capacitor selection

The selection of decoupling capacitor's value must satisfy some important constrains:

1. The value should be enough to decouple the large commutation loop inductance L_1 at the SiC MOSFET FF3MR12KM1P's current rising time t_r.

$$C_1 \gg \frac{0.2 \cdot t_r^2}{L_1} \tag{A. 2.5}$$

2. During the active cut-off switching scheme, the LF oscillation is triggered by the voltage slope at $t = 0$, when the IGBT is on.

$$i_{cf}(t) = \frac{\Delta V}{\sqrt{\frac{L_1}{C_f}}} \cdot \sin(\omega_1 t) \tag{A. 2.6}$$

$$v_{cf}(t) = -\Delta V \cdot \cos(\omega_1 t) + \frac{V_{DC}}{2} \tag{A. 2.7}$$

With

$$\Delta V = \frac{V_{DC}}{2} - V_{cf0} \tag{A. 2.8}$$

In cased of unbalanced DC link voltage,

$$\Delta V = V_{DC1} - V_{DC2} \tag{A. 2.9}$$

At time $t = t_2$, SiC MOSFET is turned off, the LF oscillation is triggered again with the current slope. The voltage and current of the decoupling capacitor at this moment can be modeled:

$$i_{cf}(t) = \pm IL \cdot \cos(\omega_1(t - t_2)) - \frac{V_{cf}\big|_{t=t_2} - \frac{V_{DC}}{2}}{\sqrt{\frac{L_1}{C_f}}} \cdot \sin(\omega_1(t - t_2)) \tag{A. 2.10}$$

$$v_{cf}(t) = \pm IL \cdot \sqrt{\frac{L_1}{C_f}} \cdot \sin\big(\omega_1(t - t_2)\big) + \left(V_{cf}\big|_{t=t_2} - \frac{V_{DC}}{2}\right) \cdot \cos(\omega_1(t - t_2)) + \frac{V_{DC}}{2} \tag{A. 2.11}$$

From (A. 2.7) the maximum possible capacitor voltage at t_2:

$$V_{cfmax}\big|_{t_2} = V_{DCmax} - V_{cf0} \tag{A. 2.12}$$

Since the worst-case scenario for the MOSFET switching is at $V_{DCmax}/2$, in this case, the initial capacitor voltage should be:

$$V_{cf0} \leq \frac{V_{DCmax}}{2} \tag{A. 2.13}$$

From equation (A. 2.11), the maximum voltage of the capacitor at all time t:

$$V_{cfmax} = \sqrt{IL^2 \frac{L_1}{C_f} + \left(\frac{V_{DCmax}}{2} - V_{cf0}\right)^2} + \frac{V_{DCmax}}{2} \tag{A. 2.14}$$

To protect the SiC half-bridge from the over voltage,

$$V_{cfmax} \leq V_{SOA} \tag{A. 2.15}$$

$$0 \le L_1 \cdot \frac{IL^2}{C_f} \le \left(V_{SOA} + V_{cf0} - V_{DCmax}\right)\left(V_{SOA} - V_{cf0}\right) \quad \text{(A. 2.16)}$$

$$0 \le V_{SOA} + V_{cf0} - V_{DCmax} \quad \text{(A. 2.17)}$$

From (A. 2.13), (A. 2.17), the limit for the initial capacitor voltage $V_{cf0}$is:

$$V_{DCmax} - V_{SOA} \le V_{cf0} \le \frac{V_{DCmax}}{2} \quad \text{(A. 2.18)}$$

The drifting voltage of the capacitor should not exceed the limit in equation (A. 2.18). In case of unbalanced DC link voltage, each half of the DC link voltage should be limited in range of:

$$V_{DC_{max}} - V_{SOA} \le \frac{V_{DC1,2}}{2} \le \frac{V_{DC_{max}}}{2} \quad \text{(A. 2.19)}$$

When the unbalanced is out of this range, the switching should be disable to avoid overvoltage of SiC MOSFET. From equation (A. 2.15), the capacitor value should be:

$$C_f \ge \frac{L_1 \cdot IL^2}{\left(V_{SOA} + V_{cf0} - V_{DCmax}\right)\left(V_{SOA} - V_{cf0}\right)} \quad \text{(A. 2.20)}$$

In case of unbalanced DC link voltage

$$C_f \ge \frac{L_1 \cdot IL^2}{\left(\frac{V_{DCmax}}{2} - V_{SOA}\right)^2 - \Delta V_{max}^2} \quad \text{(A. 2.21)}$$

With ΔV_{max} is the maximum difference between the upper and lower DC voltages.

In this application, if $V_{DCmax} = 1800V$, $V_{SOA} = 1200V$, $L_1 = 115nH$, $IL = 450A$

$$600V \le V_{cf0} \le 900V \quad \text{(A. 2.22)}$$

Choosing the initial capacitor voltage at half of nominal DC link voltage $V_{cf0} = 750V$,

$$C_f \ge 613nF \quad \text{(A. 2.23)}$$

3. The upper limit of the capacitor value is defined by the maximum current that IGBT can handle. From equation (A. 2.10), the peak current possibly going through the IGBT is:

$$IL^2 + \frac{C_f \cdot \left(\frac{V_{DCmax}}{2} - V_{cf0}\right)^2}{L_1} \leq I_{IGBTmax}^2 \quad \text{(A. 2.24)}$$

$$C_f \leq \frac{L_1 \cdot (I_{IGBTmax}^2 - IL^2)}{\left(\frac{V_{DCmax}}{2} - V_{cf0}\right)^2} \quad \text{(A. 2.25)}$$

In case of unbalanced DC link voltage,

$$C_f \leq \frac{L_1 \cdot (I_{IGBTmax}^2 - IL^2)}{(\Delta V_{max})^2} \quad \text{(A. 2.26)}$$

With ΔV_{max} is the maximum difference between the upper and lower DC voltages.

If $I_{IGBTmax} = 1200A$ is the repetitive peak collector current of the IGBT FF60012KT4 [69], in case of V_{cf0} is at 750V and maximum DC link voltage, the capacitor value is:

$$C_f \leq 5520\ nF \quad \text{(A. 2.27)}$$

The capacitor value in (A. 2.23) and (A. 2.27) is the estimated value. In the real circuit, there is resistances in the resonance circuit which attenuate the oscillation amplitude. It is possible to measure the real maximum voltage and maximum current of decoupling capacitor in one fundamental cycle of load current like in Figure A. 2.6 to have more reference when selecting decoupling capacitor value.

4. During the starting-up of the inverter all the switches are off, $V_{cf0} = 0$. To avoid overvoltage and current on the MOSFET and IGBT, the initial charging process for the decoupling capacitor must be applied. In this process, T11, T21 are on and the DC link is slowly increased from zero to nominal voltage. After the charging process is finished, the switching can be enabled.
5. Finally, it's crucial to recognize that the capacitor's value is constrained by its internal resistance, often referred to as ESR (Equivalent Series Resistance), which causes the capacitor to heat up during operation. In situations where a larger capacitor is used, a

higher RMS current flows through the capacitor, to prevent overheating, the capacitor should have low ESR and good cooling conditions. Figure A. 2.6 illustrates the current waveform of the decoupling capacitor during the active cut-off switching scheme, as measured from an oscilloscope over one fundamental cycle. Notably, when C_f is set to 1000nF, the RMS current reaches 57Arms. This value exceeds the capability of a typical snubber film capacitor, which is limited by its RMS current handling capacity to less than 30A, as indicated in reference [28].

6. Because the capacitor is in the SiC MOSFET commutation loop, its internal inductance ESL (Equivalent Series inductance), should be as small as possible. In this hybrid ANPC, a special conduction cooled capacitor like in the Figure A. 2.7 is recommended. Due to limitation in supplier and available value, the capacitor 1320nF-1000V is selected, which has the ESL = 3nH, ESR = 0.8mΩ, and can handle current up to 600 Arms. The voltage and current of the capacitor during switching can be seen in the Figure A. 2.8.

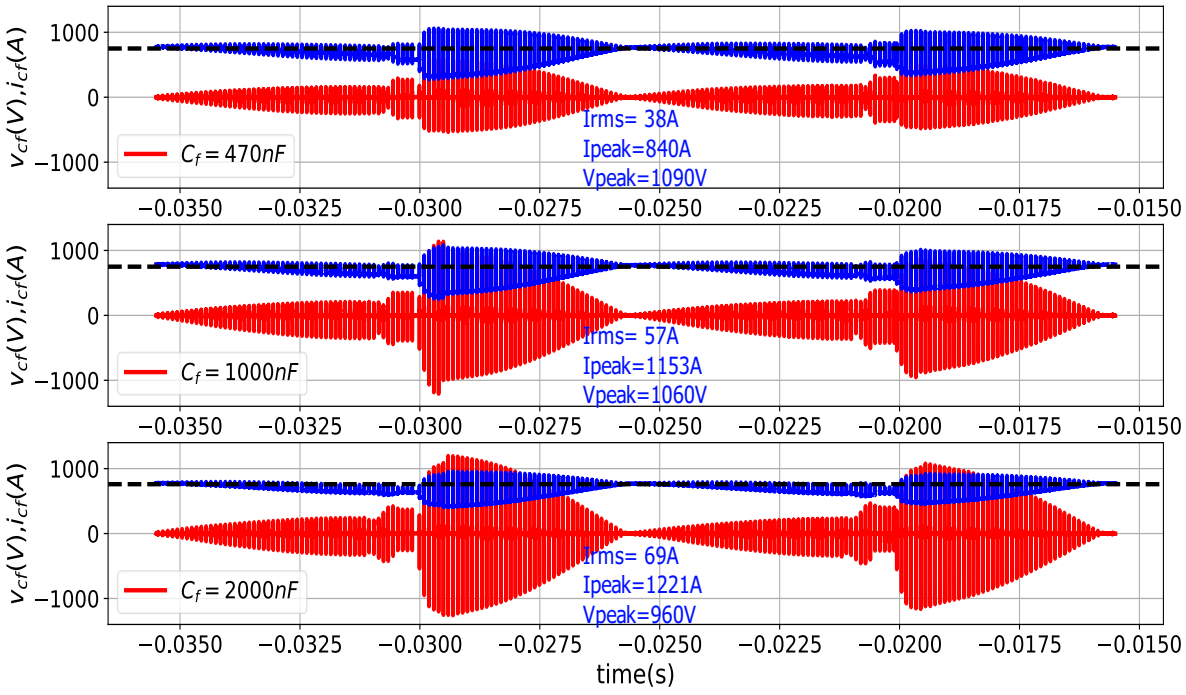


Figure A. 2.6: *Film capacitor's voltage and current waveform in one fundamental cycle, V_{DC} = 1500V, IL(rms) = 300A at different capacitor values.*

Figure A. 2.7: *Conduction cooled capacitors are recommended for the decoupling capacitor [59].*

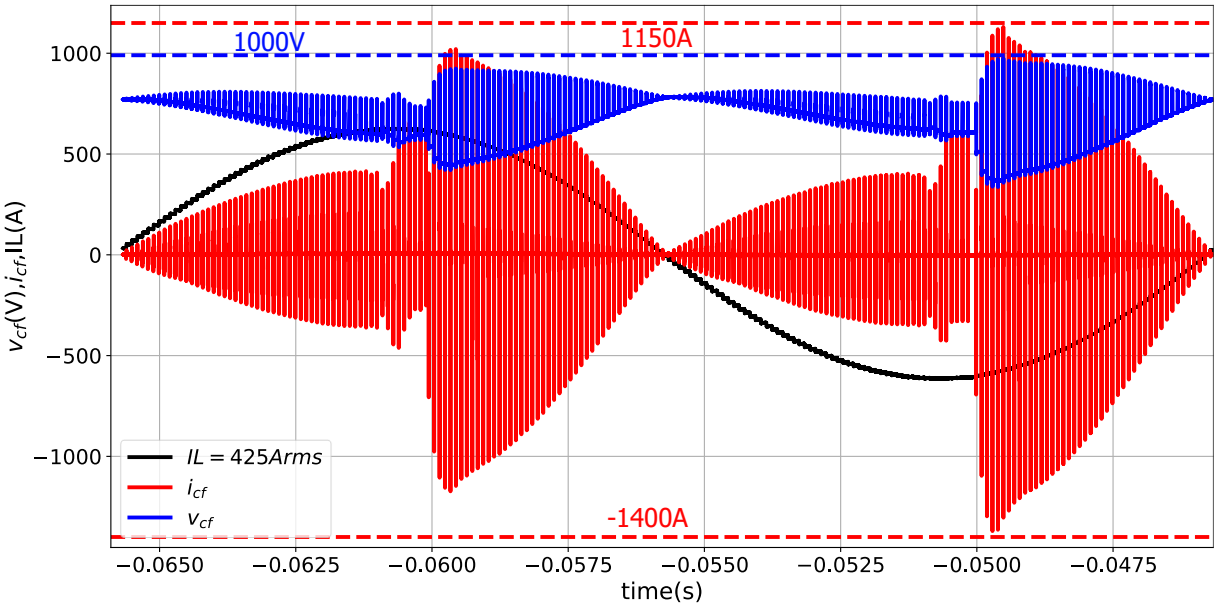


Figure A. 2.8: *Voltage and current of decoupling capacitor C_f = 1320nF during switching at ILmax = 625A, V_{DC} =1500V.*

A.2.6 Ferrite cores selection

In this ANPC, due to the small gap between the modules and the busbar, there is no T35 material core at this specified size is available for this set up. The dual ferrite cores 74270118 from Würth elektronik are used. The cores' material is soft ferrite NiZn. The dual cores position can be seen in Figure A. 2.9.

A.2.7 SiC MOSFET Gate driver design

The gate driver for the SiC MOSFET has 3 main parts which are designed separately: isolation gate power supply, gate driver, the active clamping like the Figure A. 2.9.

The design of the driver circuit starting with the calculation of the maximum gate current which is need to drive the MOSFET. Because at the input gate of the MOSFET is the capacitor, the simplified gate circuit is an RC circuit like in the Figure A. 2.10a. The peak current of an RC circuit in this case can be calculated as:

$$I_{gpeak} = \frac{V_{gson} - V_{gsoff}}{R_g + R_{gint}} \qquad \text{(A. 2.28)}$$

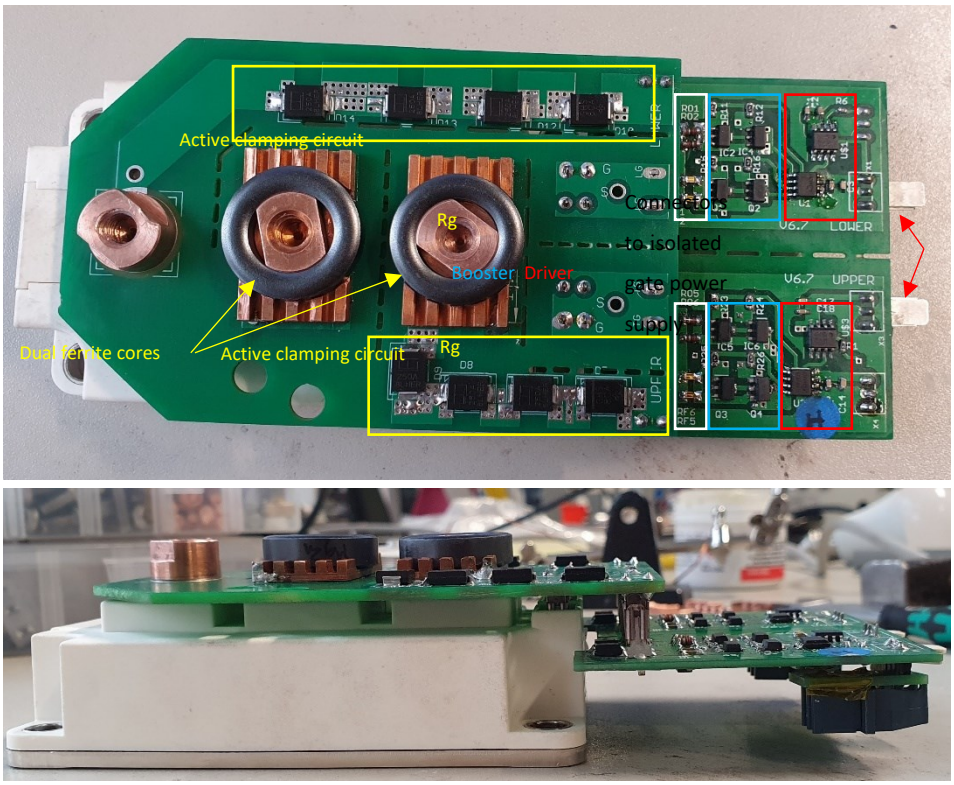


Figure A. 2.9: *Gate driver and its assembly with the SiC MOSFET module.*

The smaller gate resistance R_g is used the larger the peak of the gate current I_{gpeak} is. In this hybrid ANPC application, the SiC MOSFET can be switched at the lowest R_{gon} = 0 Ω. According to the datasheet of FF3MR12KM1P [109], the internal gate resistance is 1Ω. When the turn-on gate voltage is +15V and the turn-off gate voltage is -5, the gate current peak possibly is 20A.

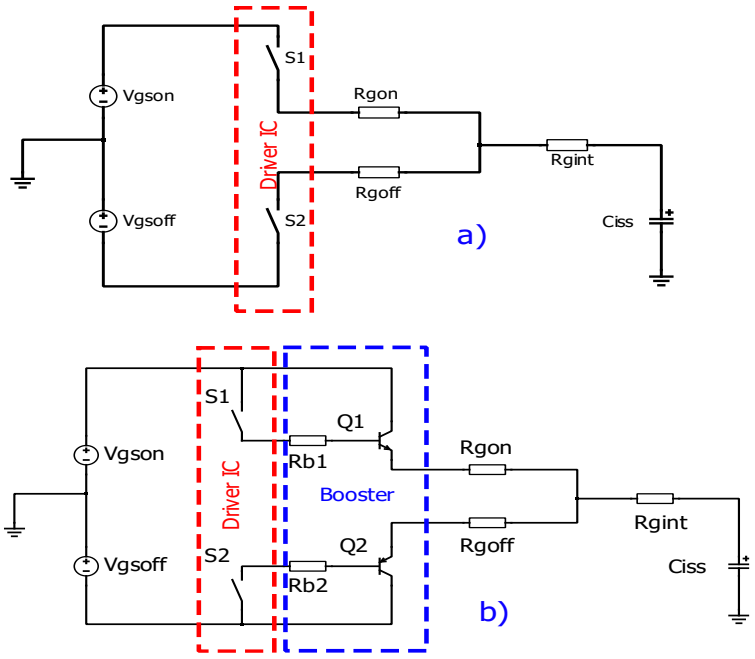


Figure A. 2.10: *The equivalent gate circuit of the MOSFET. Rgint, Ciss is the internal gate resistor and the input capacitor of the MOSFET module. a) without booster, b) with booster (dashed blue line).*

To able to provide the high peak current output, the external current booster stage is use together with the driver IC like in the Figure A. 2.10b. The external booster is the high speed NPN and PNP which have sufficient high peak current. The implement of the external booster also benefits the advanced active clamping installation which will be mention later in this appendix.

A.2.7.1 Advanced active clamping circuit

During the current falling phase of the MOSFET's the turn-off process, its channel is acting as a controlled current source [36]. The channel current can be modeled as a function of the MOSFET transconductance g_{fs}, gate voltage v_{gs} and the threshold voltage V_{th}:

$$i_{ds}(t) = g_{fs}\left(v_{gs}(t) - V_{th}\right) \tag{A. 2.29}$$

$$\frac{di_{ds}}{dt} = g_{fs} \cdot \frac{dv_{gs}}{dt} \tag{A. 2.30}$$

If the $v_{ds}(t)$ is larger than the TVS's breakdown voltage, there is a breakdown current $i_z(t)$ added to the gate current $i_g(t)$. The gate voltage at the chip's terminal at that time is:

$$v_{gs}(t) = V_{gsoff} + R_{goff} \cdot (i_g\,(t) + i_z\,(t)) \qquad \text{(A. 2.31)}$$

Replace (A. 2.31) to (A. 2.30):

$$\frac{di_{ds}}{dt} = g_{fs} \cdot R_{goff} \cdot \left(\frac{di_g}{dt} + \frac{di_z}{dt}\right) \qquad \text{(A. 2.32)}$$

Before the TVS's breakdown, $\frac{di_z}{dt}$ is zero due to the fact that $i_z = 0$, after the TVS's breakdown, $\frac{di_z}{dt} > 0$ and $\frac{di_g}{dt} < 0$. As a result, the sum $\frac{di_{ds}}{dt}$ is slowed down. The more overvoltage is, the faster $\frac{di_z}{dt}$ becomes. Consequently $\frac{di_{ds}}{dt}$ is slower and the overvoltage is clamped. This is the behavior of the conventional active clamping which can be seen in the Figure A. 2.11.

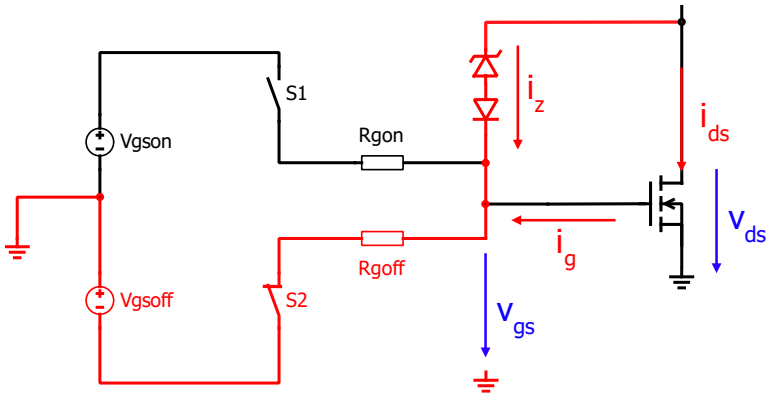


Figure A. 2.11: *Conventional active clamping.*

There is another way to slow down $\frac{di_{ds}}{dt}$ during the overvoltage. From the equation (A. 2.30), $\frac{dv_{gs}}{dt}$ can be directly manipulated by turning off Q2 and turning on Q1 of the booster like in Figure A. 2.12. The method is called advanced active clamping [81]. When the TVS is breakdown, the breakdown current i_{z2} turn off Q2 and turn on Q1 of the booster, the current i_{z1} is used to boost the charging of Q2's the output capacitor to rise v_{gs} faster.

In the conventional active clamping, the turn-off switch S2 of the gate driver has to carry both the breakdown current and the gate current, which increases the stress of the driver IC.

The problem can be solved with the advanced active clamping concept, the benefit is especially valuable for the continuous operation, where the driver is switched thousand times per second.

In this application, to limit the overvoltage under 1200V, three 1.5SMC250A and one SMCJ188A are used which provides the breakdown voltage from 920V to 1020V. It is well known that the breakdown voltage is temperature dependent [80, 98] and can be linearized as:

$$V_{bdTj} = V_{bd25}\left(1 + \alpha_T\left(T_j - 25\right)\right) \tag{A. 2.33}$$

The expected breakdown voltage of the TVS diodes at 150°C according to the equation (A. 2.33) is 1030V-1148V with $\alpha_T = 0.1\%$ [98]. As it can be seen in Figure A. 2.13 that the clamped voltage at 75°C which is higher 60V than at 25°C.

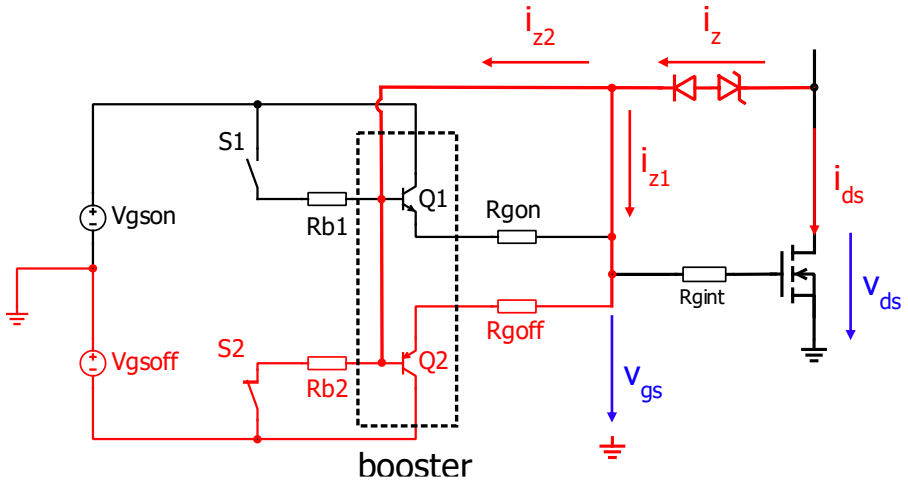


Figure A. 2.12: *Advanced active clamping.*

It should be noticed that the peak voltage during the clamping is higher than the actual clamped voltage (Figure A. 2.13) because of the oscillation circuit created by the inductance of the clamping circuit and the diodes' junction capacitors. To improve the effective of the active clamping circuit, the inductance between the TVS diodes and the protected MOSFET should be minimized. To achieve the low inductance clamping circuit, the active clamping PCB is mounted directly on the the SiC MOSFET module like in Figure A. 2.14. Because the PCB trace can't handle a large load current up to 300Arms, the special copper terminals are made and soldered directly on the PCB circuit. The terminals let the load current go through the module and the PCB traces give the feedback voltage to the TVS diodes.

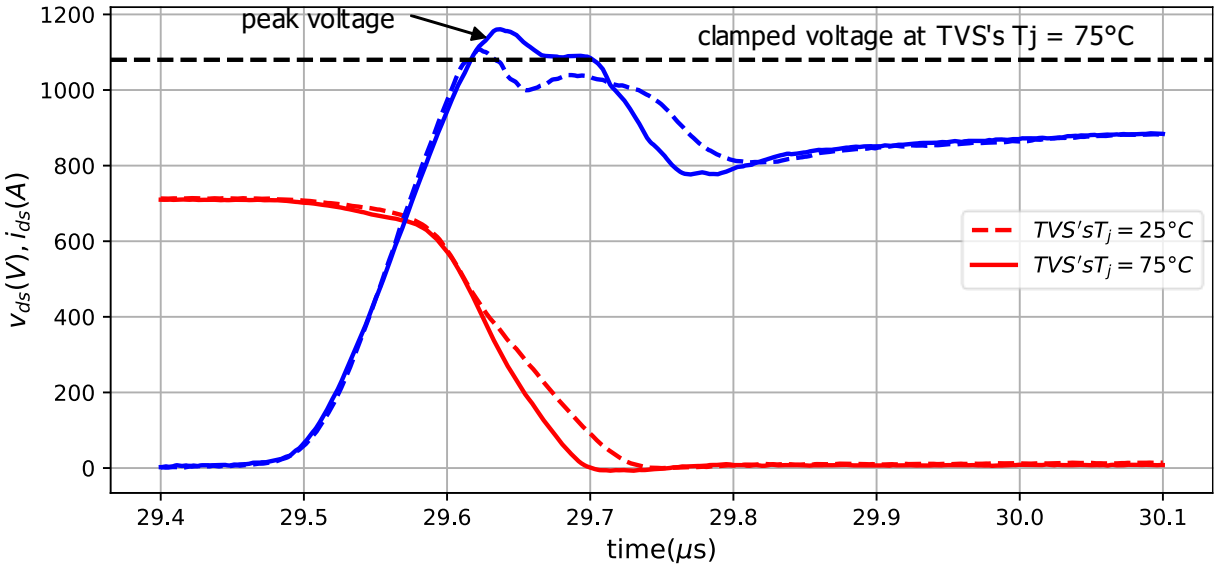


Figure A. 2.13: *The breakdown voltage of the TVS diodes increases with temperature which, TVS' breakdown voltage at 25°C = 1000V (solid lines), TVS' breakdown voltage at 75°C = 1060V (dashed line).*

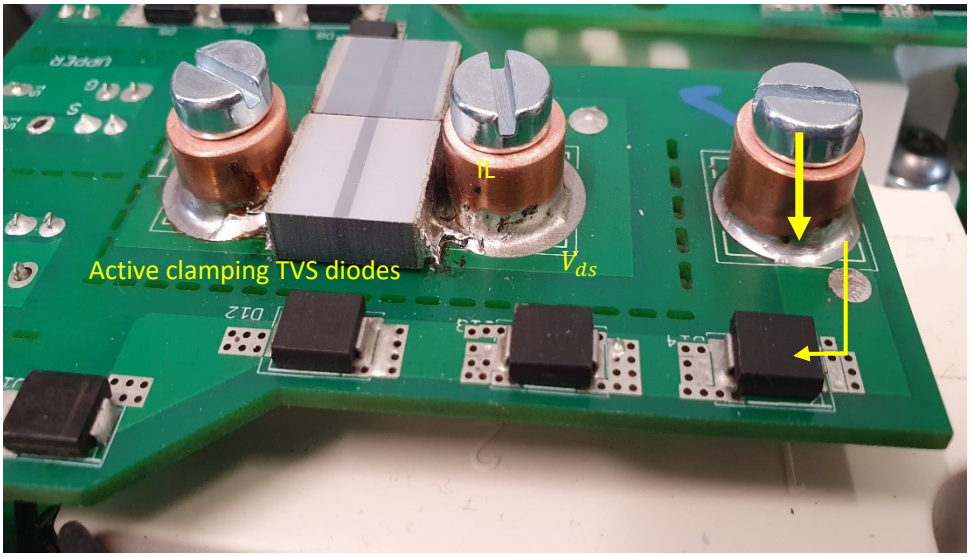


Figure A. 2.14: *Active clamping PCB with the special copper terminals allow high load current passing through and give the feedback voltage to the TVS diodes.*

A.2.7.2 Gate driver isolated power supply

Because there is limited space under the busbar and the modules, the gate drivers' power supply is separated. To save the design time and effort, the commercial isolated gate driver

power supply is used. To select the proper power supply, some parameters should be considered:

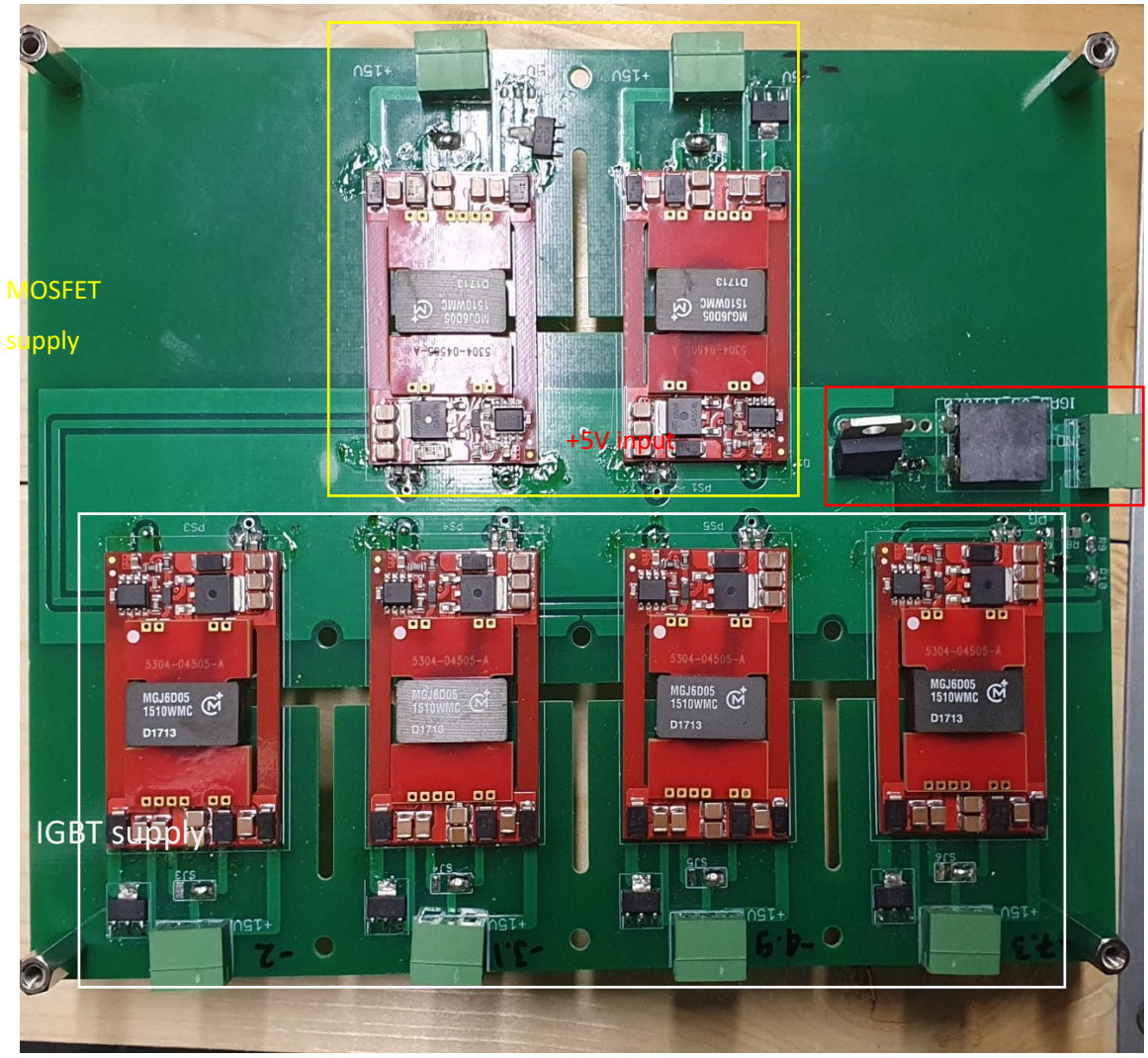


Figure A. 2.15: *The gate driver isolated power supply for SiC MOSFET and IGBT.*

Table A. 2.6: *Gate driver isolation power supply MGJ6D241505WMC parameters [53].*

Input voltage (V)	Ouput voltage (V)	Power (W)	Continuous Isolation Voltage (V_{DC})	dv/dt immunity (V/ns)	Rated output current (mA)
5	+15/-5	6	3000	80	300

The power of the gate driver circuit can be calculated based on the SiC MOSFET total gate charge Q_{gate} and the switching frequency f_{sw}. In this application, FF3MR12KM1P has

the total gate charge is $1\mu C$ [109] and it is switched at 10kHZ, the gate driver loss is estimated around 0.2W

$$P_{drive} = Q_{gate} \cdot f_{sw} \cdot \left(V_{gson} - V_{gsoff}\right) \qquad \text{(A. 2.34)}$$

The isolation of the power supply should be sufficient for continuous DC link voltage up to 900V. Apart from that, the coupling capacitor between primary and secondary of the power supply should be low enough to have the good du/dt immunity. In this application, the MGJ6D241505WMC is used.

A.2.8 Inverter controller unit

The inverter has 3 main boards: Analog board, control board and optical switching board which can be seen in the Figure A. 2.16.

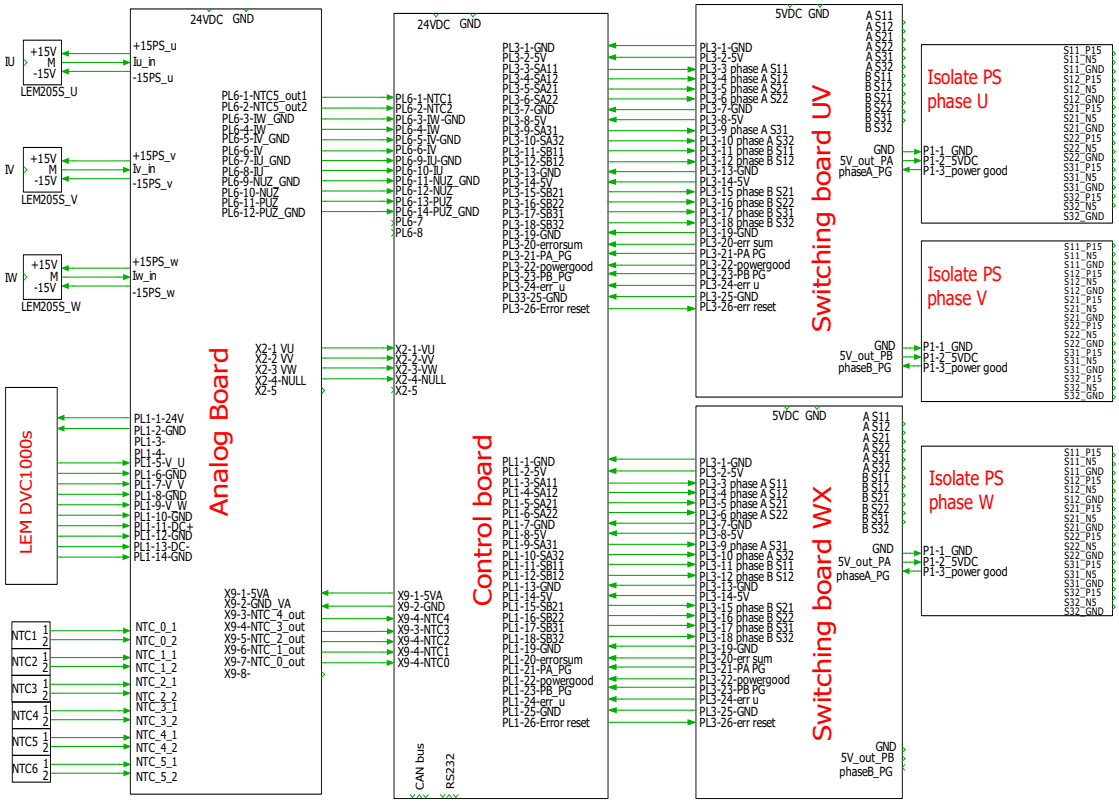


Figure A. 2.16: *Inverter's controller unit wiring diagram.*

The control board is a DSP TMS320F28335 interfacing with a FPGA Xilinx Spartan 3. The board is originally designed by ISLE. The main functions of the board are:

- Provides: 6x3 switching signals, implements the control algorithm.
- Measures: 3 phases voltage and currents, DC link voltage and heatsink temperatures
- Communicates: the collected data are sent online to the user over the optical CAN bus. Apart from that, there is also one RS232 for programming the DSP and FPGA and one RS232 port for offline debug.

To improve the immunity against the common mode noises, the main board power supplies and all the I/O are isolated and filtered.

A.2.8.1 Controller board

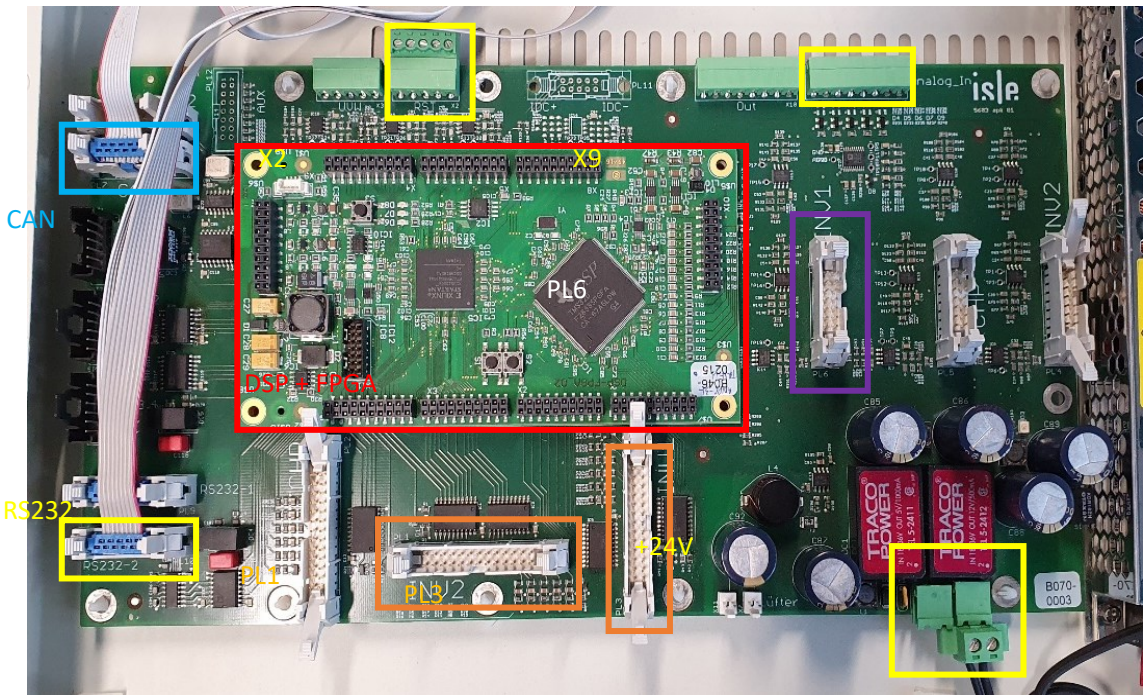


Figure A. 2.17: *The inverter's controller board.*

A.2.8.2 Analog board

The analog board collects data from:

- Three phases voltages and DC+, DC- from the voltage sensors LEM DVC-1000. Because of the high voltage inputs, the sensors are assembled in separated board in a plastic box. The output signals are sent to the analog board and processed in the control board.

- Three phases currents from the current sensors LEM-205. The signals are sent to the analog board and processed in the control board
- The heatsinks' temperatures from the NTCs. The signals are collected on the analog board and processed in the control board.

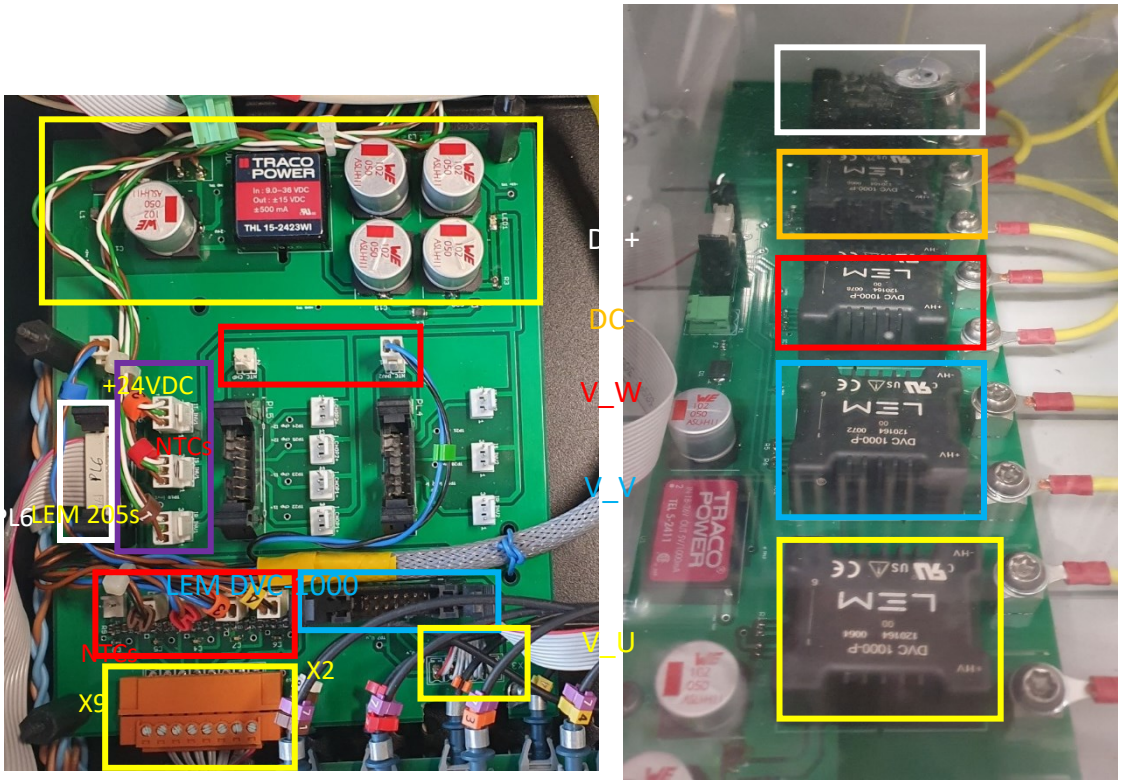


Figure A. 2.18: *The inverter's analog board and LEM DVC-1000 board.*

A.2.8.3 Optical switching board

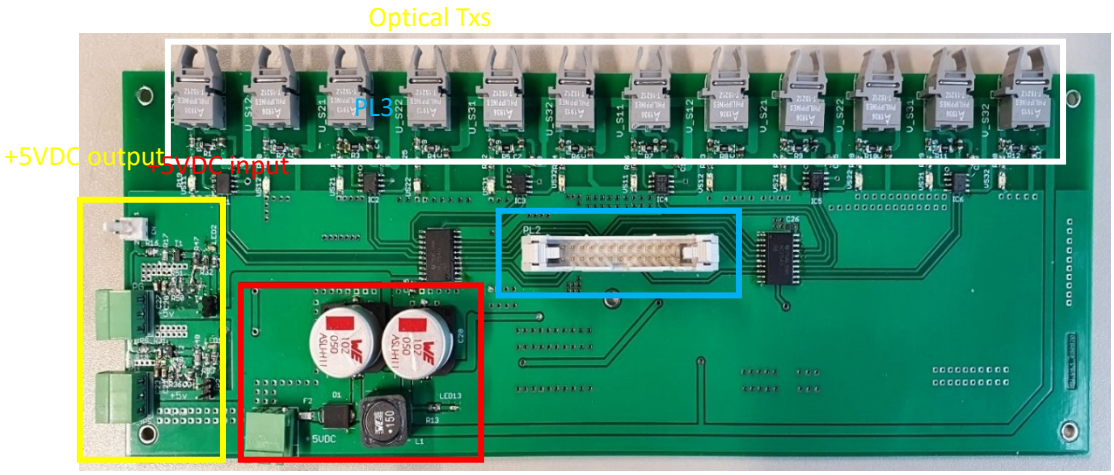


Figure A. 2.19: *The inverter's optical switching board.*

The optical switching board converts the switching signals from the control board to the optical signals which trigger the gate drivers. The board also provides filtered +5V_{DC} output to the isolated gate driver power supply. There is a power good signal on the board which is a daisy chain feedback the gate driver power supplies' status. If one of the driver supplies is failed, the controller will be notified.

A.2.8.4 Controller panel assembly

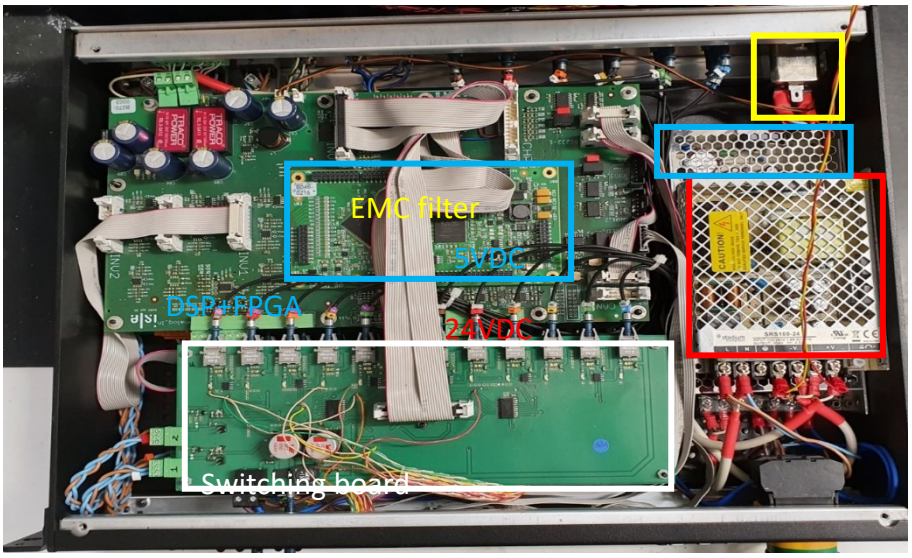


Figure A. 2.20: *Internal of the controller panel.*

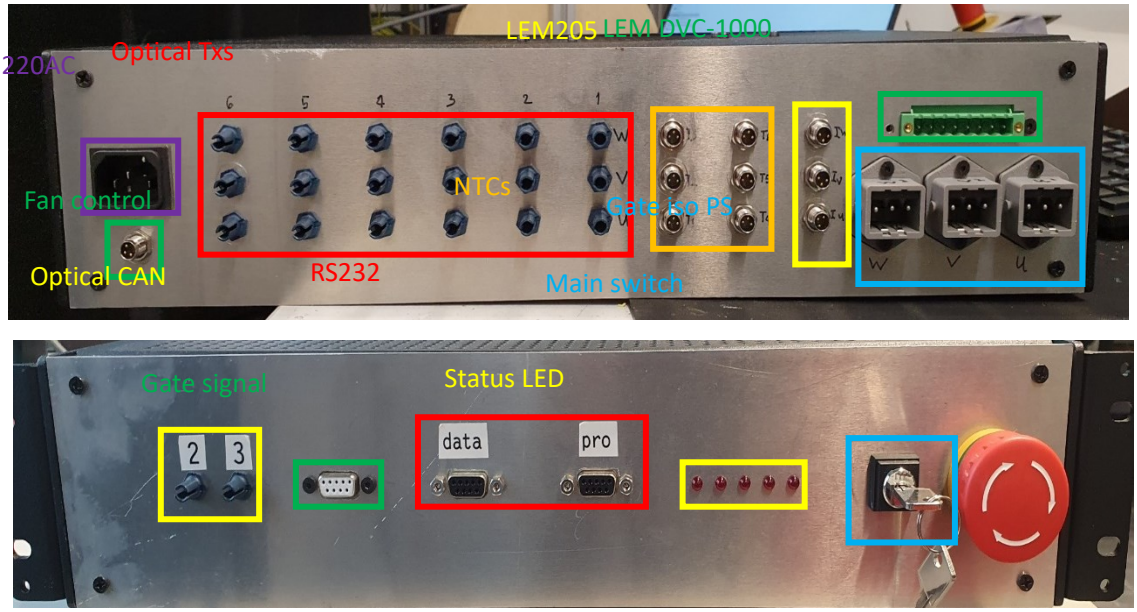


Figure A. 2.21:*The back and front of the controller unit.*

All the boards of the controller unit are assembled in a 19" panel like in the Figure A. 2.20, Figure A. 2.21. The $220V_{AC}$ input is filtered by the EMC filter before suppling for the 5 V_{DC} and 24 V_{DC}. There are some other components on the controller unit such as:

- The optical CAN bus converter board used for online data communication. The user's commands are sent on this optical communication link (Figure A. 2.22).
- The fan controller monitors the heatsinks' temperatures and turn on and off the cooling fan.
- Gate signals monitor port provides a direct measurement of the switching signals to the oscilloscope.
- The status LEDs indicates the current status of the inverter.

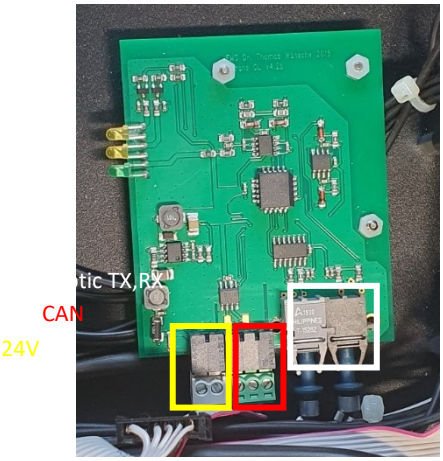


Figure A. 2.22: *Optical CAN bus converter board.*

A.2.9 LC filter design

The filter inductor L_{inv} is fabricated by STS with the parameters are displayed in the Table A. 2.7. The LC filter assembly is shown in the Figure A. 2.23.

Table A. 2.7: *Filter inductor parameters.*

Inductive	$140\mu H$
Peak current	450A
Nominal current	300Arm @ 50Hz

isolation	1500V
Maximum temperature	70°C

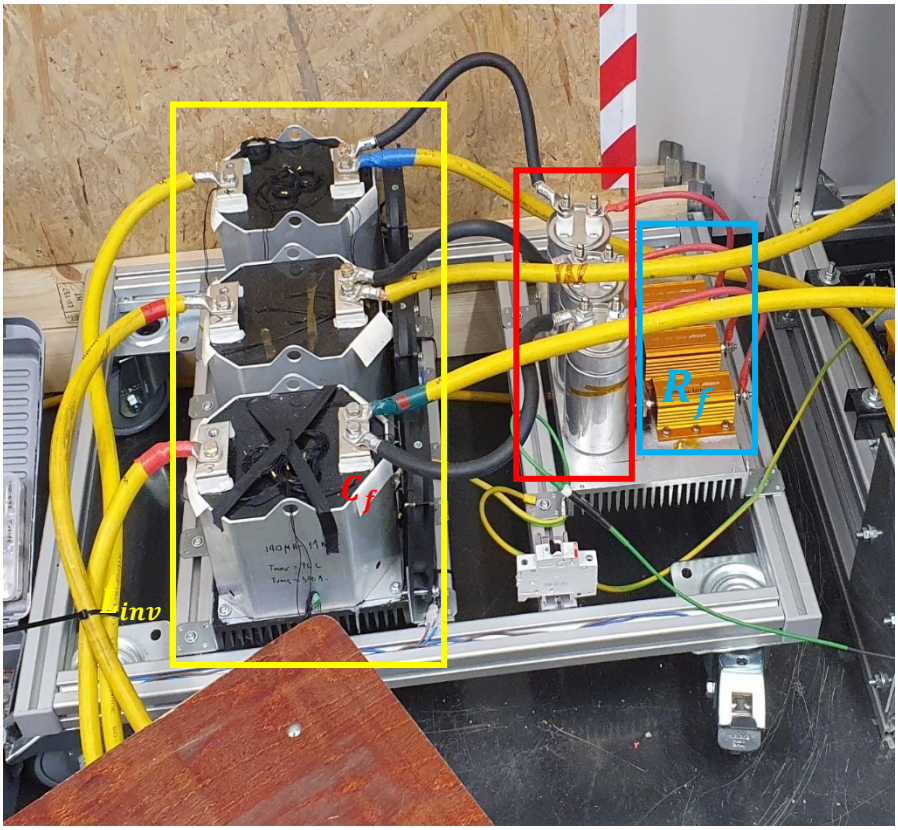


Figure A. 2.23: *LC filter assembly.*

A.2.10 Inverter assembly

Figure A. 2.24, Figure A. 2.25 depict a complete three phases assembly of the hybrid ANPC. In order to mitigate the common mode noise produced by the inverter, an EMI filter is installed at the high voltage DC supply input as shown in Figure A. 2.25.

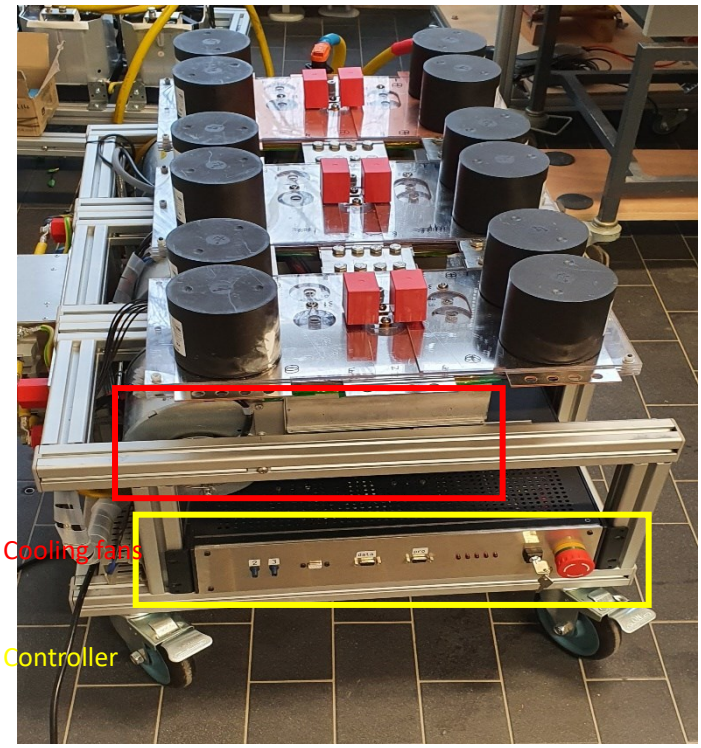


Figure A. 2.24: *Three phases assembly of the hybrid ANPC-front side.*

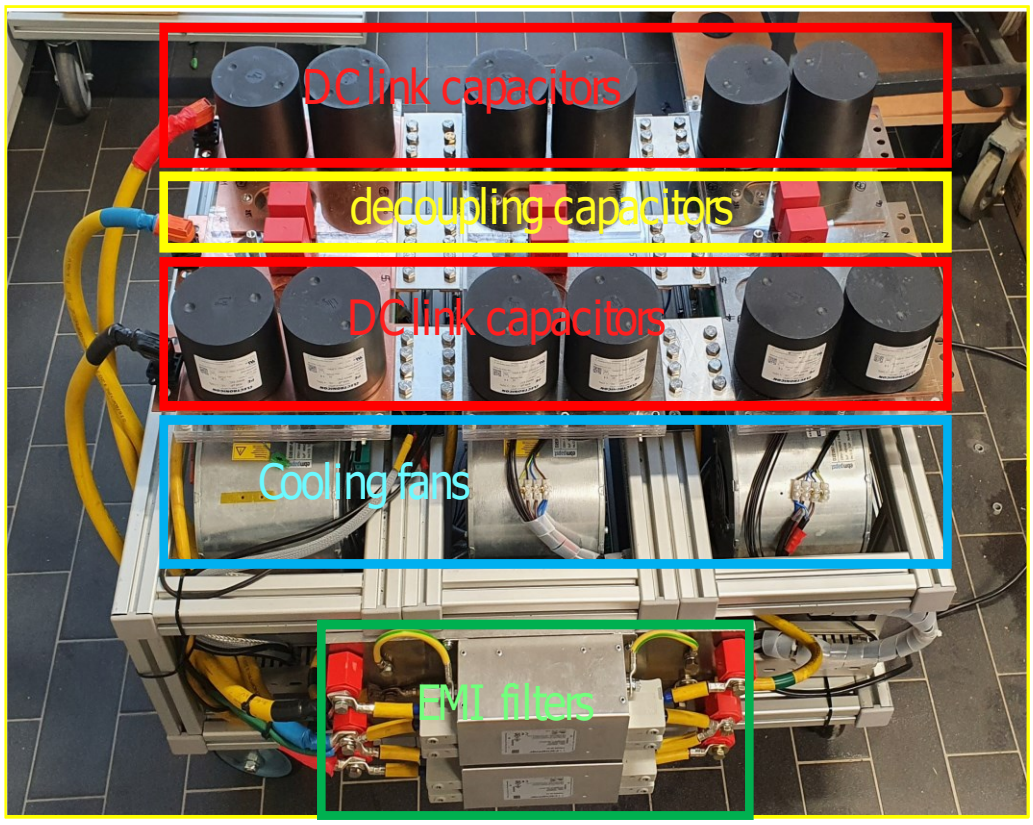


Figure A. 2.25: *Three phases assembly of the hybrid ANPC-back side.*

A.2.11 Software design

The hybrid ANPC software consists of three primary components: FPGA firmware, DSP firmware, and a graphical user interface (GUI) designed for Windows. The FPGA handles the implementation of the PWM scheme and state machine, while the DSP manages tasks such as the inverter current control and data acquisition. Facilitating communication between the DSP and GUI is the CAN bus, which enables the DSP to receive commands and transmit data to the GUI.

A.2.11.1 FPGA

The FPGA firmware is responsible for executing two key functions: generating PWM signals and operating the state machine for the active cut-off switching scheme. The DSP transmits the reference voltage to the FPGA via an external memory interface featuring a 32-bit data bus and a 10-bit address bus. This interface enables direct reading and assignment of variables within the DSP that correspond to their counterparts in the FPGA's logic [50].

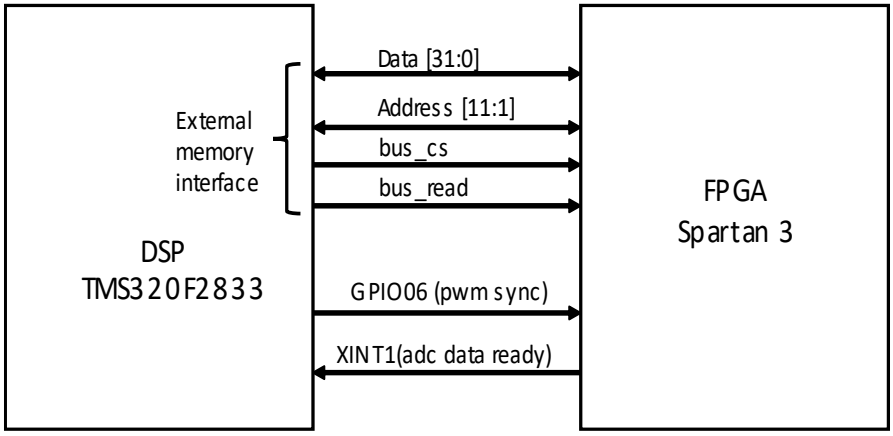


Figure A. 2.26: *The DSP and FPGA parallel communication.*

A.2.11.2 PWM generator

The PWM generator employs the phase disposition technique, having two synchronized triangle carriers (v_{cr1}, v_{cr2}) that are in phase. The reference voltage (v_{ref}) is then compared with these carriers and zero voltage (Figure A. 2.27). This comparison results in four potential scenarios for the reference voltage's position. These cases, outlined in Table A. 2.8, correspond to distinct 3-bit output vectors (PZN). Each value of the PZN set represents one of the four switching states of the inverter: P, ZP, ZN, and N.

Table A. 2.8: *The output of the PWM generator and the inverter's switching states.*

	P	Z	N	Switching states
$V_{ref} > V_{cr1}$	1	1	1	P
$V_{cr1} \geq V_{ref} > 0$	0	1	1	ZP
$0 \geq V_{ref} > V_{cr2}$	0	0	1	ZN
$V_{cr2} \geq V_{ref}$	0	0	0	N

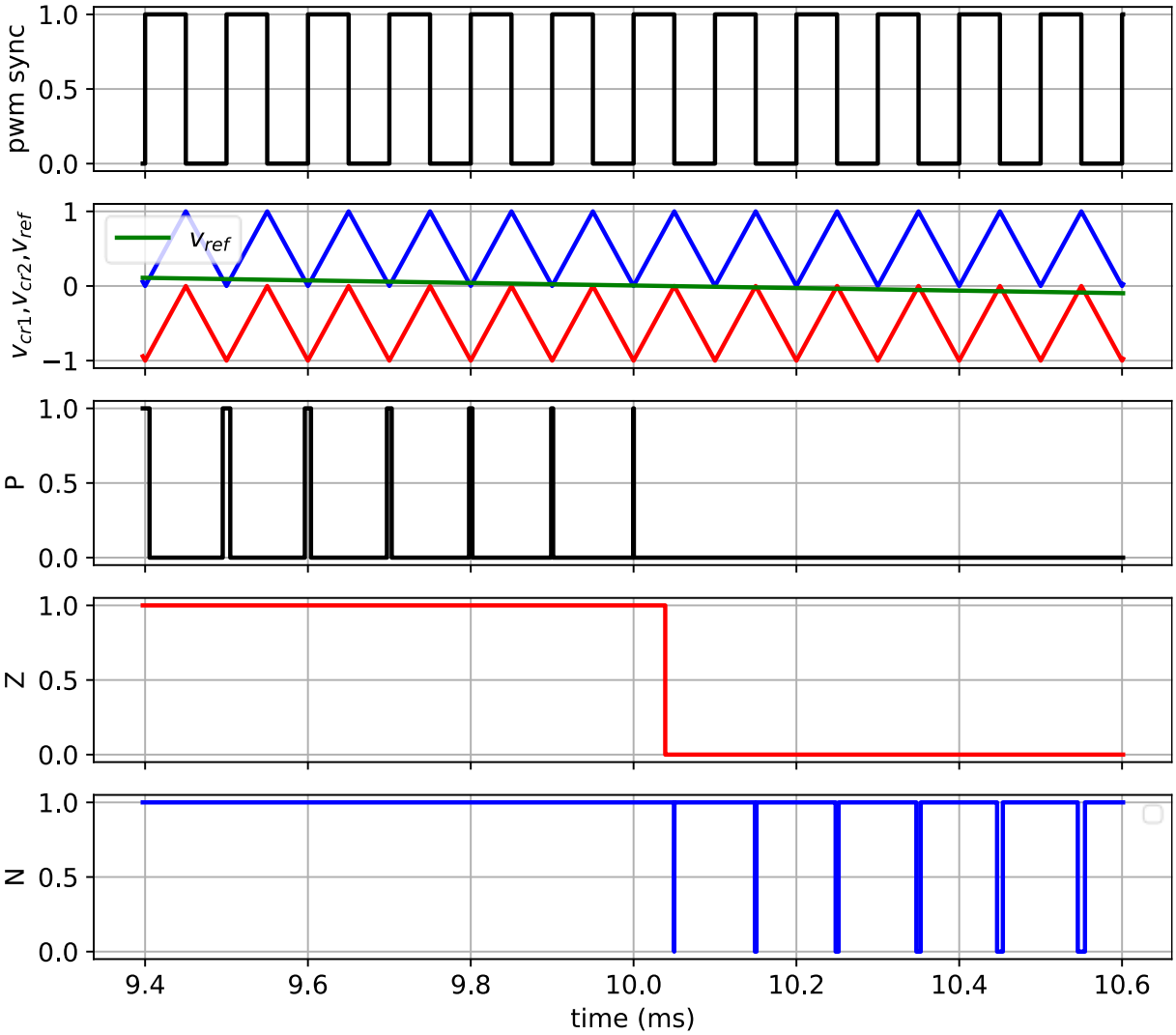


Figure A. 2.27: *The PWM generator signals are synchronized with the DSP's ADC sampling frequency (pwm sync).*

The waveforms of the carriers are generated in synchronization with the ADC sampling signal from the DSP, which is indicated by the "pwm sync" signal. The sampling rate is double the switching frequency.

A.2.11.3 Active cut-off switching scheme's state machine

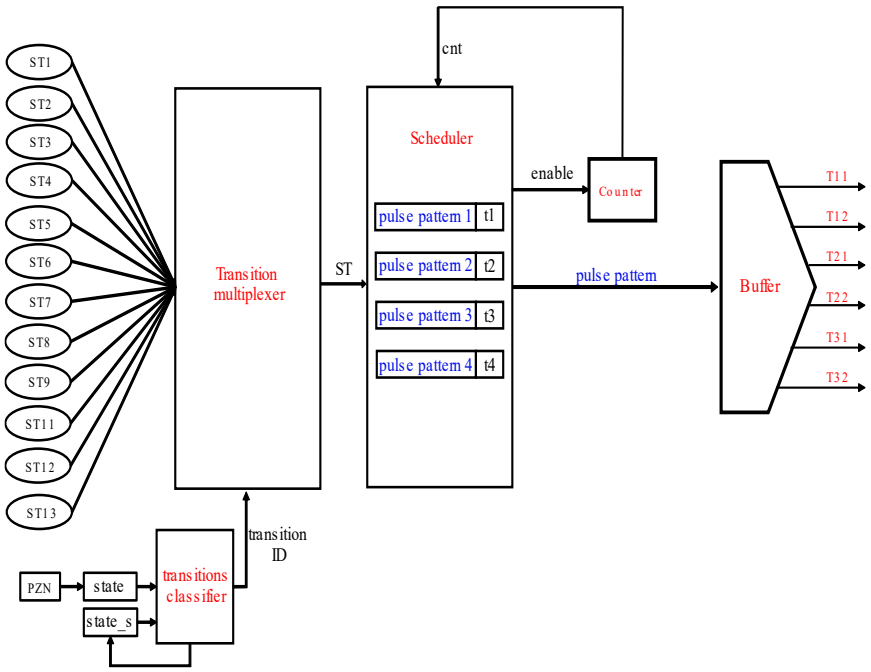


Figure A. 2.28: *Active cut-off switching scheme's state machine block diagram.*

The input of the state machine is a 3-bit vector known as PZN, which serves as the state machine's trigger. This value is assigned to the variable "state" allowing it to be compared with its prior state "state_s" by the transition classifier. This comparison plays a pivotal role in discerning the transition ID from the pool of 12 diverse transitions (labeled ST1 through ST12). In addition, there exists a 13th state named ST13, dedicated to the initial charging sequences of the decoupling capacitor.

The transition ID, once identified, becomes the input for the transition multiplexer. This multiplexer is responsible for selecting the appropriate transition (ST), which is then routed to the scheduler. Each transition state (ST) encompasses a series of pulse patterns and their corresponding timings. The scheduler employs a singular counter to meticulously load these pulse patterns in alignment with their designated timings. As a harmonizing step, the pulse patterns are subsequently channeled into a buffer, which provides synchronized triggers to the switches.

Upon the completion of a transition, the updated state is stored in the "state_s" variable. Simultaneously, the counter is deactivated, and waiting for the new state.

To avoid the glitches at the output signals, all the input, output signals and components in the state machine are synchronized with the system clock.

A.2.12 State machine VDHL code

```
entity state_machine is
  generic(
  t1: integer := 14;
  t2: integer := 62;
  t3: integer := 162;
  t4: integer := 228;
  t5: integer := 129;
  t6: integer := 212
  );
 ------------------------------------------------
   Port ( PZN : in  STD_LOGIC_VECTOR (3 downto 1);
                      clk_bus : in  STD_LOGIC;
                      enable : in  STD_LOGIC;
                      SW11    : out STD_LOGIC;
                      SW12    : out STD_LOGIC;
                      SW21    : out STD_LOGIC;
                      SW22    : out STD_LOGIC;
                      SW31    : out STD_LOGIC;
                      SW32    : out STD_LOGIC
                      --debug1  : out STD_LOGIC_VECTOR (15 downto 0);
                      --debug2  : out STD_LOGIC_VECTOR (15 downto 0)
```

```
                        );
end state_machine;
architecture Behavioral of state_machine is
-------------------------- State definition ---------------------------------------------
---- P: Vref > Vcr1, Z: Vref > 0, N: Vref > Vcr2
----------------State of the machine
constant VP: STD_LOGIC_VECTOR (3 downto 1) := "111";--PZN
constant VN: STD_LOGIC_VECTOR (3 downto 1) := "000";--PZN
constant ZP: STD_LOGIC_VECTOR (3 downto 1) := "011";--PZN
constant ZN: STD_LOGIC_VECTOR (3 downto 1) := "001";--PZN
-----------------------------------------------------------------------------------------
signal state:STD_LOGIC_VECTOR (3 downto 1):= ZN;
signal state_s:STD_LOGIC_VECTOR (3 downto 1):= ZN;
signal st_out: STD_LOGIC_VECTOR (6 downto 1) := "010010";
signal st_cnt: integer range 0 to 50000 := 0; --- state timer counter
signal enable_s :STD_LOGIC :='0';
signal cnt_en:STD_LOGIC :='0';              --- state timer counter enable
signal enable_rst: STD_LOGIC_VECTOR(1 downto 0);
signal st_ID :integer range 0 to 14 := 0;           ---state ID
-----------------------------------------------------------------------------------------
begin
counter : process
begin
  wait until rising_edge(clk_bus); --- may be change to process sensitive list
                        if( cnt_en = '1') then
                                st_cnt <= st_cnt + 1;
```

```
                else
                        st_cnt <= 0;
                end if;
end process counter;
-------------------------------------------------------
State_machine_loop : process
begin
wait until rising_edge(clk_bus);
state <= PZN;
--------------------------------State change detection -----------------
  if (cnt_en = '0') then --- check if the counter is free
        if ( (state_s = ZP) and (state = VP)) then     -- 1 from ZP to VP
                        st_ID <= 1;
                        cnt_en <= '1';
        elsif ( (state_s = VP) and (state = ZP)) then  -- 2 from VP to ZP
                        st_ID <= 2;
                        cnt_en <= '1';
    elsif ( (state_s = ZN) and (state = VN)) then  -- 3 from ZN to VN
                        st_ID <= 3;
                        cnt_en <= '1';
        elsif ( (state_s = VN) and (state = ZN)) then  -- 4 from VN to ZN
                        st_ID <= 4;
                        cnt_en <= '1';
        elsif ( (state_s = VP) and (state = VN)) then -- 5 from VP to VN
                st_ID <= 5;
                cnt_en <= '1';
```

```
elsif ( (state_s = VN) and (state = VP)) then -- 6 from VN to VP
        st_ID <= 6;
        cnt_en <= '1';
elsif ( (state_s = ZP) and (state = VN)) then -- 7 from ZP to VN
        st_ID <= 7;
        cnt_en <= '1';
elsif ( (state_s = VN) and (state = ZP)) then -- 8 from VN to ZP
        st_ID <= 8;
        cnt_en <= '1';
  elsif ( (state_s = ZP) and (state = ZN)) then -- 9 from ZP to ZN
        st_ID <= 9;
  elsif ( (state_s = ZN) and (state = ZP)) then --10 from ZN to ZP
        st_ID <= 10;
elsif ( (state_s = ZN) and (state = VP)) then -- 11 from ZN to VP
        st_ID <= 11;
        cnt_en <= '1';
elsif ( (state_s = VP) and (state = ZN)) then -- 12 from VP to ZN
        st_ID <= 12;
        cnt_en <= '1';
end if;
end if;
---------- capacitor charging at enable rising edge
if ( (enable_s ='0') and (enable = '1') )  then -- rising edge of enable turn on capacitor charging
        st_ID <= 13;
        cnt_en <= '1';
```

```
  end if;
   enable_s <= enable;
----------------------------state output-------------------------------------
case st_ID is
  when 1 =>       --   from ZP -> VP:    001001 -> 100010
            if ((st_cnt >= 1)and (st_cnt < t1)) then
                  st_out <= "101000"; --turn on S11,turn of S32
            elsif ((st_cnt >= t1)and (st_cnt < t2 )) then
                  st_out <= "100000"; -- turn off S21
            elsif ((st_cnt >= t2) and (st_cnt < t3 )) then
                  st_out <= "100010"; -- turn on S31
            elsif (st_cnt >= t3) then
                  cnt_en <= '0'; --disable counter
                  state_s <= VP; -- record current state
            end if;
  when 2|5 =>    --  from VP -> ZP: 100010 -> 001001
                  if ((st_cnt >= 1)and (st_cnt < t1)) then
                        st_out <= "101000"; --turn on S21, turn off S31
                  elsif ((st_cnt >= t1)and (st_cnt < t2 )) then
                        st_out <= "001000"; -- turn off S11
                  elsif ((st_cnt >= t2) and (st_cnt < t3 )) then
                        st_out <= "001001"; -- turn on S32
                  elsif (st_cnt >= t3) then -- after tun delay time allow new state
                        cnt_en <= '0';--disable counter
                        state_s <= ZP; -- record current state
                  end if;
```

```
when 3 =>   --  from ZN -> VN : 010010 -> 000101
                    if ((st_cnt >= 1)and (st_cnt < t1)) then
                        st_out <= "010100"; -- turn on S22, turn off T31
                    elsif ((st_cnt >= t1)and (st_cnt < t2 )) then
                        st_out <= "000100"; -- turn off S12
                    elsif ((st_cnt >= t2) and (st_cnt < t3 )) then
                        st_out <= "000101"; -- turn on S32
                    elsif (st_cnt >= t3) then -- after tun delay time allow new state
                        cnt_en <= '0';--disable counter
                        state_s <= VN; -- record current state
                    end if;
when 4|6 => --  from VN -> ZN:  000101 ->010010
                if ((st_cnt >= 1)and (st_cnt < t1)) then
                    st_out <= "010100"; --turn on S12,turn off S32
                elsif ((st_cnt >= t1)and (st_cnt < t2 )) then
                    st_out <= "010000"; -- turn off S22
                    elsif ((st_cnt >= t2) and (st_cnt < t3 )) then
                    st_out <= "010010"; -- turn on S31
                elsif (st_cnt >= t3) then -- after tun delay time allow new state
                    cnt_en <= '0'; --disable counter
                    state_s <= ZN; -- record current state
                end if;
when 7 =>    --  ZP -> VN :   001001 -> 000101
                if ((st_cnt >= 1) and (st_cnt < t5)) then
                    st_out <= "000001"; --turn off S21
                elsif ((st_cnt >= t5)-and (st_cnt < t6  )) then
```

```
                st_out <= "000101"; --turn on S22
            elsif (st_cnt >= t6) then
                cnt_en <= '0';--disable counter
                state_s <= VN;-- record current state
            end if;
    when 8 =>    --  VN -> ZP :   000101 -> 001001
            if ((st_cnt >= 1)and (st_cnt < t5)) then
                st_out <= "000001"; --turn off S22
            elsif ((st_cnt >= t5)and (st_cnt < t6  )) then
                st_out <= "001001"; --turn on S21
            elsif (st_cnt >= t6) then
                cnt_en <= '0';--disable counter
                state_s <= ZP;-- record current state
            end if;
   when 9  =>    -- ZP to ZN
        state_s <= ZP;-- record current state ( stay on ZP = ZN state wait for new state
  when 10 =>    -- from ZN to ZP
        state_s <= ZN;-- record current state ( stay on ZN = ZP state wait for new state)

 when 11 =>   --  ZN -> VP : 010010 -> 100010
        if ((st_cnt >= 1)and (st_cnt < t5)) then
            st_out <= "000010"; --turn off S12
        elsif ((st_cnt >= t5)and (st_cnt < t6)) then
            st_out <= "100010"; --turn on S11
        elsif (st_cnt >= t6) then
                    cnt_en <= '0';--disable counter
```

```
                    state_s <= VP;-- record current state
                end if;
when 12 =>   --  VP -> ZN : 100010 -> 010010
                if ((st_cnt >= 1)and (st_cnt < t5)) then
                    st_out <= "000010"; --turn off S11
                elsif ((st_cnt >= t5)and (st_cnt < t6)) then
                    st_out <= "010010"; --turn on S12
                elsif (st_cnt >= t6) then
                    cnt_en <= '0';--disable counter
                    state_s <= ZN;-- record current state
                end if;
when 13 =>   -- decoupling capacitor charging process
 if ((st_cnt >= 1)and (st_cnt < 10000)) then  --  turn off all switch and wait for 60us
        st_out <= "000000"; --turn off S11
 elsif ((st_cnt >= 10000)and (st_cnt < 11000)) then
        st_out <= "000001"; --turn on S12
 elsif ((st_cnt >= 11000)and (st_cnt < 41000)) then
        st_out <= "100001"; --turn on S11
 elsif ((st_cnt >= 41000)and (st_cnt < 45000)) then
        st_out <= "001001"; --turn on S11  -- return to ZP state
 elsif (st_cnt >= 45000) then
        cnt_en <= '0';--disable counter
        state_s <= ZP;-- record current state
 end if;
        when others => null
 end case;
```

```
    end process State_machine_loop;
-------------------------------------------------------------------------------------------------------------
    output_process : process
    begin
     wait until rising_edge(clk_bus);
      SW11 <= st_out(6);
      SW12 <= st_out(5);
      SW21 <= st_out(4);
      SW22 <= st_out(3);
      SW31 <= st_out(2);
      SW32 <= st_out(1);
    end process output_process;
    end Behavioral;
```

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